BD663474

240RGB × 320-Dot 1-Chip Driver IC with Built-in RAM

for 262,144-Color TFT-LCD Panel

Rev. 0.03
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Overview

The BD663474 is 1-chip solution for TFT-LCD in 262,144 colors. It incorporates source driver, gate driver, and power supply circuits to drive a color TFT liquid crystal display. This 1-chip solution can display 240RGB×320-dot graphics on the panel.

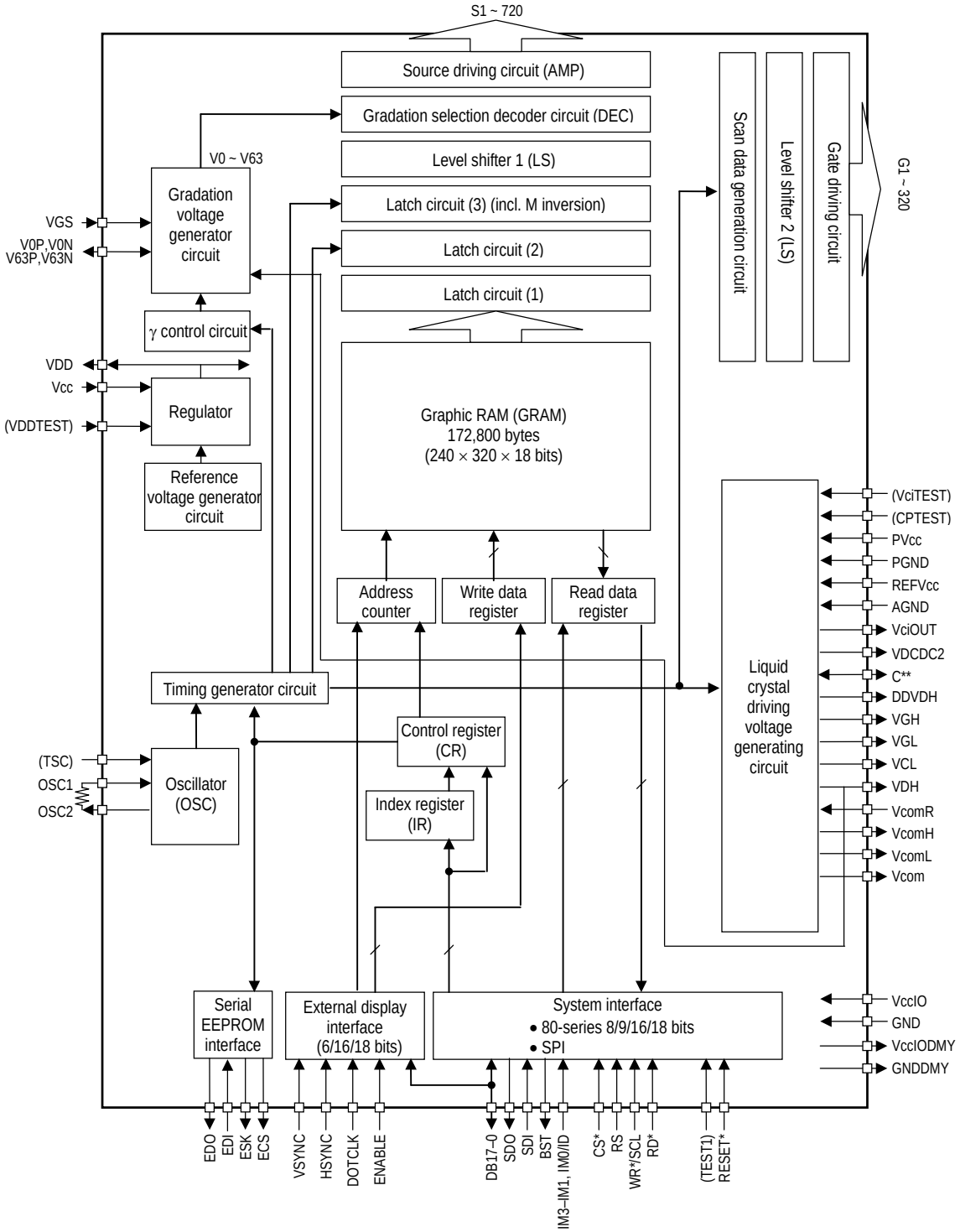
High-speed 8-, 9-, 16-, 18-bit bus interfaces and serial peripheral interface that are used as the system interface with the microcomputer enable efficient data transfer as well as high-speed rewriting of graphic RAM. The BD663474 is also equipped with 6/16/18 bits RGB-I/F (VSYNC, HSYNC, DOTCLK, and ENABLE) to interface with moving images.

The BD663474 supports functions to reduce power consumption of the LCD system. The system interface can be operated with a low voltage up to 1.65V, which can minimize the power consumption attributed to charging/discharging of the LCD module wiring and can transfer data at high-speed as well. The BD663474 incorporates a voltage follower circuit to generate a liquid crystal drive voltage as well as another voltage follower circuit to drive large-volume liquid crystal for every output. These circuits can be built into the optimum setting by the software, taking the picture quality and the power consumption into account. Functions such as the partial display and the standby function supported by the BD663474 enable precise power management by software. These features make this LSI an optimum LSI for medium or small-sized portable products with color displays such as WWW browser-equipped digital cellular phones or small PDAs, where long battery life is a major concern.

Features

- Drives 262,144 TFT-color 240RGB × 320 dot graphics display
- Display type: a-Si TFT, IPS
- Structure for TFT-display retention volume: Cst structure
- System interface: Built-in high-speed 8/9/16/18-bit bus interfaces and serial peripheral interface (SPI)
- Contains interface to support display of moving pictures
  - Built-in 6/16/18-bit RGB-I/F (VSYNC, HSYNC, DOTCLK, ENABLE)
- Contains interface for serial EEPROM
- Built-in function for high-speed burst RAM write
- Window address function enables writing to rectangular RAM address area
- Power supply voltage
  - Interface power supply: VccIO = 1.65V to 3.3V
  - Power supply for internal logic circuits: Vcc = 2.5V to 3.3V
  - Power supply for analog circuits: PVcc, REFVcc = 2.5V to 3.3V
- Output voltage of built-in step-up circuit
  - DDVDH – GND = 4.5 to 6.0V (for source driving and Vcom driving)
  - VGH – GND = 9.0 to 13.0V (for gate driving)
  - VGL – GND = –4.0 to –5.0V (for gate driving)
  - VCL – GND = 0 to –VciOUT (V) (for Vcom driving)
- Output voltage
  - VciOUT – GND = 2.0 to PVcc (V) (Reference voltage for step-up circuits)
  - VDCDC2 – GND = 4.0 to DDVDH (V) (Reference voltage for step-up circuit 2)
  - Vcom – GND (for TFT common electrode)
  - VcomH = 2.5 to (DDVDH – 0.5) V (High voltage of Vcom)
  - VcomL = (VCL + 0.5) to 0.5V (Low voltage of Vcom)
  - VcomH – VcomL (Vcom amplitude) = 6V max.
- Employment of low power consumption architecture
  - Power saving functions such as deep standby mode
  - Partial liquid crystal drive of 2 screens at any position
  - Built-in circuit to step-up liquid crystal drive voltage up to 8 times
  - Control of DC current on bleeder resistance by voltage follower circuit for liquid crystal drive power source
  - Step-up circuit control function, operational amplifier control function
- Built-in RAM capacity: 172,800 bytes (240 × 320 × 18bits)
- Built-in LCD drive circuit: 720-output Source Driver, 320-output Gate Driver
- Built-in oscillator, reset of hardware/software available

Block Diagram



Terminal Functions

1. Control signals

<table>
<tr><th>Signal name (Interface voltage)</th><th>No. of terminals</th><th>Input/ Output</th><th>Connected to</th><th>Functions</th><th>When not used</th></tr>
<tr><td>RESET*
(VccIO/GND)</td><td>1</td><td>Input</td><td>External reset circuit</td><td>Used to enter the hardware-reset signal.
Initializes LSI at “Low”.
Power-on reset is required when turning on power supply.</td><td>—</td></tr>
<tr><td>IM3-1,
IM0/ID
(VccIO/GND)</td><td>4</td><td>Input</td><td>GND
or
VccIO</td><td>Used to select interface mode with MPU.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU interface mode</th><th>DB terminal used</th></tr>
<tr><td>IM3</td><td>GND</td><td>GND</td><td>GND</td><td>Not selectable</td><td>—</td></tr>
<tr><td>GND</td><td>GND</td><td>GND</td><td>VccIO</td><td>Not selectable</td><td>—</td></tr>
<tr><td>GND</td><td>GND</td><td>VccIO</td><td>GND</td><td>80-series 16bit interface</td><td>DB17-10, DB8-1</td></tr>
<tr><td>GND</td><td>GND</td><td>VccIO</td><td>VccIO</td><td>80-series 8-bit interface (Big-endian)</td><td>DB17-10</td></tr>
<tr><td>GND</td><td>VccIO</td><td>GND</td><td>ID</td><td>Serial peripheral interface 1</td><td>SDI, SDO</td></tr>
<tr><td>GND</td><td>VccIO</td><td>VccIO</td><td>GND</td><td>Not selectable</td><td>—</td></tr>
<tr><td>GND</td><td>VccIO</td><td>VccIO</td><td>VccIO</td><td>80-series 8-bit interface (Little-endian)</td><td>DB17-10</td></tr>
<tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>Not selectable</td><td>—</td></tr>
<tr><td>VccIO</td><td>GND</td><td>GND</td><td>VccIO</td><td>Not selectable</td><td>—</td></tr>
<tr><td>VccIO</td><td>GND</td><td>VccIO</td><td>GND</td><td>80-series 18-bit interface</td><td>DB17-10</td></tr>
<tr><td>VccIO</td><td>GND</td><td>VccIO</td><td>VccIO</td><td>80-series 9-bit interface</td><td>DB17-9</td></tr>
<tr><td>VccIO</td><td>VccIO</td><td>GND</td><td>ID</td><td>Serial peripheral interface 2</td><td>SDI, SDO</td></tr>
<tr><td>VccIO</td><td>VccIO</td><td>VccIO</td><td>*</td><td>Not selectable</td><td>—</td></tr>
</table>
* When the serial peripheral interface is selected, IM0 is used for the ID of device codes. SDO outputs during the data output halt become VccIO level in the serial peripheral interface 1 mode and Hi-Z in the serial peripheral interface 2 mode respectively.</td><td>—</td></tr>
<tr><td>CS*
(VccIO/GND)</td><td>1</td><td>Input</td><td>MPU</td><td>Chip select signal.
"Low" : Selected (Access enabled)
"High" : Unselected (Access disabled)
This terminal is common to 80-series and serial peripheral interfaces.</td><td>—</td></tr>
<tr><td>RS*
(VccIO/GND)</td><td>1</td><td>Input</td><td>MPU</td><td>Register select signal for 80-series bus interface.
"Low" : Index register / Status register
"High" : Control register
Not used in serial peripheral interface mode.</td><td>VccIO</td></tr>
<tr><td>WR*/SCL
(VccIO/GND)</td><td>1</td><td>Input</td><td>MPU</td><td>Write strobe signal in 80-series bus interface mode. Writes data at "Low". Synchronizing clock signal in serial peripheral interface mode.</td><td>—</td></tr>
<tr><td>RD*
(VccIO/GND)</td><td>1</td><td>Input</td><td>MPU</td><td>Read strobe signal in 80-series bus interface mode. Reads data at "Low". Not used in serial peripheral interface mode.</td><td>VccIO</td></tr>
</table>

Signal name (Interface voltage)	No. of terminals	Input/ Output	Connected to	Functions	When not used
DB17-0 (VccIO/GND)	18	Input/ Output	MPU	18-bit bi-directional data bus in 80-series bus interface mode. See below for terminals used in each mode. 8-bit interface : DB17-10 9-bit interface : DB17-9 16-bit interface : DB17-10, 8-1 18-bit interface : DB17-0 18-bit RGB data bus in RGB interface mode. See below for terminals used in each mode (RIM setting). 6-bit interface : DB17-12 16-bit interface : DB17-13, 11-1 18-bit interface : DB17-0 Fixed to "VccIO" or "GND" level when not used.	GND or VccIO
SDI (VccIO/GND)	1	Input	MPU	Serial data input terminal in serial peripheral interface mode. Loads data on the rising edge of SCL. Fixed to "VccIO" or "GND" level when not used.	GND or VccIO
SDO (VccIO/GND)	1	Output	MPU	Serial data output terminal in serial peripheral interface mode. Outputs data on the falling edge of SCL.	open
VSYNC (VccIO/GND)	1	Input	MPU	Frame synchronization signal in RGB interface mode. This is a "Low" active signal, but can be used as a "High" active signal by changing the register setting. Set to inactive when the RGB interface is not used.	GND or VccIO
HSYNC (VccIO/GND)	1	Input	MPU	Line synchronization signal in RGB interface mode. This is a "Low" active signal, but can be used as a "High" active signal by changing the register setting. Set to inactive when the RGB interface is not used.	GND or VccIO
DOTCLK (VccIO/GND)	1	Input	MPU	Dot clock signal in RGB interface mode. The timing of data loading is set at the rising edge. This is a "High" active signal, but can be used as a "Low" active signal by changing the register setting. Set to inactive when the RGB interface is not used.	GND or VccIO
ENABLE (VccIO/GND)	1	Input	MPU	Data enable signal in RGB interface mode. "Low" : Selected (Access enabled) "High" : Unselected (Access disabled) This is a "Low" active signal, but can be used as a "High" active signal by changing the register setting. Set to inactive when the interface is not used.	GND or VccIO
BST (VccIO/GND)	1	Output	MPU	Outputs pulses indicating start of the blank period (front porch). When writing data in synchronization with display scan, this can be used as a trigger signal.	open
ECS (Vcc/GND)	1	Output	EEPROM	Chip select signal. “High”: Selected (Access enabled) “Low”: Unselected (Access disabled)	open
ESK (Vcc/GND)	1	Output	EEPROM	Synchronizing clock signal.	open
EDI (Vcc/GND)	1	Input	EEPROM	Serial data input terminal. Loads data on the rising edge of ESK signal. Fixed to “Vcc” or “GND” level when not used.	GND or Vcc
EDO (Vcc/GND)	1	Output	EEPROM	Serial data output terminal. Outputs data on the falling edge of ESK signal.	open

2. Oscillator and power supply

Signal name (Interface voltage)	No. of terminals	Input/ Output	Connected to	Functions	When not used
OSC1, OSC2 (VDD/GND)	1/1	Input/ Output	Oscillation resistor	Terminal to oscillate CR. Connect external resistor to this. When supplying the clock externally, use OSC1 and set OSC2 terminal to open.	—
VccIO	4	Input	Power supply	Power supply for system and RGB interfaces. VccIO: +1.65V to +3.3V	—
Vcc	6	Input	Power supply	Power supply for internal logic regulator and analog circuit. Vcc: +2.5V to +3.3V	—
REFVcc	2	Input	Power supply	Reference power supply for liquid crystal drive circuit. Voltages supplied to Vcc and REFVcc must be equal. REFVcc: +2.5V to +3.3V	—
PVcc	4	Input	Power supply	Power supply for step-up circuit. Voltages supplied to Vcc and PVcc must be equal. PVcc: +2.5V to +3.3V	—
VDD	6	Input/ Output	Stabilizing Capacitor	Power supply for internal logic. Only connect this to a stabilizing capacitor.	—
GND	6	Input	Power supply	GND for internal logic circuit and GRAM. GND = 0V	—
AGND	6	Input	Power supply	GND for analog circuit and interface except for internal logic, GRAM and step-up circuit. AGND = 0V	—
PGND	4	Input	Power supply	GND for step-up circuit. PGND = 0V	—

3. Step-up circuit and liquid crystal drive circuit

Signal name	No. of terminals	Input/ Output	Connected to	Functions	When not used
DDVDH	6	Output	Stabilizing Capacitor	Power supply for driving source driver and Vcom. This is generated by the step-up circuit 1. A capacitor is required on this pin. DDVDH: +4.5V to +6.0V	—
VGH	3	Output	Stabilizing Capacitor	Power supply for driving TFT gate driver. This is generated by the step-up circuit 2. A capacitor is required on this pin. VGH: +7.5V to +13.0V	—
VGL	3	Output	Stabilizing Capacitor	Power supply for driving TFT gate driver. This is generated by the step-up circuit 2. A capacitor is required on this pin. VGL: –4.0V to –5.0V	—
VCL	4	Output	Stabilizing Capacitor	Power supply for driving VcomL. This is generated by the step-up circuit 3. A capacitor is required in accordance with the instruction “VCOMG”. VCL: 0V to –VciOUT (V)	—
VciOUT	4	Output	Stabilizing Capacitor	Reference voltage output for step-up circuit. This is generated from internally generated reference voltage with amplitude REFVcc-GND. Voltage is controlled by the instruction “VC”. Set up the voltage output so that DDVDH, VGH, and VCL outputs are within the specified voltage. A capacitor is required in accordance with the instruction “VC”. VciOUT: +2.0V to PVcc (V)	—

Signal name	No. of terminals	Input/ Output	Connected to	Functions	When not used
VDCDC2	2	Output	Stabilizing Capacitor	Reference voltage output for step-up circuit 2. This is generated from internally generated reference voltage with amplitude REFVcc-GND. Voltage is controlled by the instruction “VRD”. Set up the voltage output so that VGH and VGL outputs are within the specified voltage. A capacitor is required in accordance with the instruction “APR”. VDCDC2: +4.0V to DDVDH (V)	—
C11+, C11-	4/4	Input/ Output	Step-up capacitor	Used for built-in step-up circuit 1. Connect a capacitor between these pins.	—
C1A+, C1A-	4/4	Input/ Output	Step-up capacitor	Used for built-in step-up circuit 1. Connect a capacitor between these pins in accordance with the instruction “CA”.	open
C21+, C21-	2/2	Input/ Output	Step-up capacitor	Used for built-in step-up circuit 2. Connect a capacitor between these pins.	—
C22+, C22-	2/2	Input/ Output	Step-up capacitor	Used for built-in step-up circuit 2. Connect a capacitor between these pins in accordance with the instruction “BT”.	open
C31+, C31-	4/4	Input/ Output	Step-up capacitor	Used for built-in step-up circuit 3. Connect a capacitor between these pins in accordance with the instruction “VCOMG”.	open
VDH	1	Output	Stabilizing Capacitor	Reference voltage output. This is generated from internally generated reference voltage with amplitude REFVcc-GND.Voltage is controlled by the instructions “VC” and “VRH”. This output is used for: (1) Source driver gradation reference voltage VDH (2) VcomH level reference voltage (3) Vcom amplitude reference voltage A capacitor is required. VDH = 3.0 to (DDVDH – 0.5) (V)	—
Vcom	4	Output	TFT common electrode	Output for TFT display common electrode. Output level ranges between VcomH and VcomL. This output inverts the polarity of the common electrode voltage. The cycle of polarity inversion is set with the register.	—
VcomH	4	Output	Stabilizing Capacitor	Vcom high level output. Voltage value is adjusted with VcomR pin. A capacitor is required on this pin. VcomH = 2.5 to (DDVDH – 0.5) (V)	—
VcomL	4	Output	Stabilizing Capacitor	Vcom low level output. Voltage value is controlled by the instruction “VDV”. Set up the voltage output so that Vcom amplitude is within the specified voltage. A capacitor is required in accordance with the register “VCOMG”. VcomL = (VCL + 0.5) to 0.5 V	—
VcomR	1	Input	Variable resistor or open	Reference voltage input for VcomH. Apply the variable resistor between VDH and GND to generate the reference voltage.	open
VGS	1	Input	GND or external resistor	Reference level for gradation voltage generator circuit. Connect external variable resistor when adjusting the level panel by panel with the source driver.	—
S1~S720	720	Output	LC panel	Signal lines to output voltage for applied liquid crystal.	open
G1~G320	320	Output	LC panel	Gate line output. • TFT ON level: VGH • TFT OFF level: VGL	open

4. Others

Signal name (Interface voltage)	No. of terminals	Input/ Output	Connected to	Functions	When not used
VccIODMY	2	Output	Input terminal	Outputs internal "VccIO" level. When adjacent input terminals are fixed at "VccIO", short-circuit these terminals.	open
GNDDMY	4	Output	Input terminal	Outputs internal "GND" level. When adjacent input terminals are fixed at "GND", short-circuit these terminals.	open
TESTD0	1	Output	open	Test pin. Set to open.	open
TESTD1	1	Output	open	Test pin. Set to open.	open
TEST1 (VccIO/GND)	1	Input	GND	Test pin. Fix to "GND".	—
VDDTEST (VccIO/GND)	1	Input	GND	Test pin. Fix to "GND".	—
CPTEST (VccIO/GND)	1	Input	GND	Test pin. Fix to "GND".	—
VciTEST (VccIO/GND)	1	Input	GND	Test pin. Fix to "GND".	—
TSC (VDD/GND)	1	Input	GND	Test pin. Fix to "GND".	—
OSC3 (VccIO/GND)	1	Output	open	Test pin. Set to open.	open
TS0 – TS8 (VccIO/GND)	9	Output	open	Test pins. Set to open.	open
TOUT1 – 3 (VccIO/GND)	3	Output	open	Test pins. Set to open.	open
RESO	1	Output	open	Test pin. Set to open.	open
VTEST	1	Output	open	Test pin. Set to open.	open
VMON	1	Output	open	Test pin. Set to open.	open
V0P, V63P	2	Input/ Output	open	Test pins. Set to open.	open
V0N, V63N	2	Input/ Output	open	Test pins. Set to open.	open
TESTA	1	Output	open	Test pin. Set to open.	open
TESTC	1	Output	open	Test pin. Set to open.	open
VAEP, VAEN	2	Output	open	Test pins. Set to open.	open
VGLDMY	4	Output	open	Outputs internal “VGL” level.	open
DMY1 – 18	18	—	—	Dummy pads.	—

Functions of Blocks

(1) System interface (MPU Interface)

The BD663474 supports two types of system interface: 80-series 18/16/9/8-bit bus interface and clock synchronous serial interface (SPI: Serial Peripheral Interface). The 8-bit bus interface corresponds to the data output from both big-endian and little-endian microcomputers. The interface mode is selected by setting the IM3-0 terminals.

The BD663474 has 16-bit registers (index register and control register) and 18-bit registers (write data register and read data register). The index register is the register to store index information from each control register and GRAM. The write data register is the register for temporarily storing data that is written to the GRAM, and the read data register is the register for temporarily storing data that is read from the GRAM. When writing data from the microcomputer to the GRAM, the data is first written to the write data register and then automatically written to the GRAM by internal operation. Data from the GRAM is read through the read data register. Therefore, data read out for the first time is invalid. Normal data is read from the second time on.

Instructions can be written consecutively because the execution time of an instruction other than starting oscillation is 0 clock cycles.

Table: Register selection (80-series bus interface)

80-series bus interface			Operation
WR*	RD*	RS	
0	1	0	Writes index to index register
1	0	0	Reads internal status.
0	1	1	Writes data to control register or GRAM (through write data register).
1	0	1	Reads GRAM through read data register.

Table: Register selection (Serial peripheral interface)

Start byte		Operation
R/W bit	RS bit	
0	0	Writes index to index register
1	0	Reads internal status.
0	1	Writes data to control register or GRAM (through write data register).
1	1	Reads GRAM through read data register.

(2) External display interface (RGB I/F, VSYNC I/F)

The BD663474 supports the RGB interface and the VSYNC interface as the external display interface for displaying moving images. When the RGB interface is selected, the display operation is synchronized with externally supplied signals (VSYNC, HSYNC, DOTCLK). The display data (DB17-0) is written in synchronization with these signals according to the data enable signal (ENABLE) to prevent flicker on the screen while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock, except for frame synchronization, which is synchronized with the VSYNC signal. Display data is written to the GRAM through the current system interface. See “External Display Interface” for details of the constraints on the speed and the method of writing to the GRAM.

Switching with the current system interface can be performed by instructions, so the optimum interface can be selected according to the display state (moving/still images). All display data written through the RGB interface is written to the internal GRAM so that data transfer is restricted to when data is updated, in order to reduce power consumption while displaying moving images.

(3) Oscillation circuit (Oscillator)

The circuit oscillates CR by just connecting an external resistance between the OSC1 and OSC2 terminals. Adjusting the external resistance varies the oscillation frequency. Select the external resistance taking the operating voltage, number of lines to be displayed, and frame frequency into consideration. This circuit can accept an externally generated operation clock. CR oscillation halts during standby mode to reduce power consumption. See “Oscillation Resistor” for details.

(4) Index register (IR)

The index register is a register to store the access information for each control register or GRAM. Switching between control register and GRAM access is defined by the index register information and the states of the RS, WR and RD terminals.

(5) Control register (CR)

The control register writes data according to the address selected by the index register and the states of the RS, WR and RD terminals. The data stored in this control register is used for display operation, GRAM access operation, internal analog circuit operation and EEPROM reading/writing operations.

(6) Write data register

The write data register is a register to temporarily store data that is written to the GRAM. External data is temporarily stored according to the control register setting value, address counter setting value, and states of the RS, WR and RD terminals before writing to the GRAM.

(7) Read data register

The read data register is a register to temporarily store data that is read from the GRAM. Temporarily stored data is output according to the control register setting value, address counter setting value and states of the RS, WR and RD terminals. For both 80-series and SPI, the read-out data of the first 16 bits or eight bits is invalid. Normal data is read from the second time on.

(8) Address counter

The address counter gives an address to the GRAM. As the address setting instruction is written to the index register, the address information is transferred from the index register to the address counter. After the data is written to the GRAM, the address counter is automatically updated plus or minus 1.

Reading data does not update the address counter. Using the window address function allows data to be written to the specified rectangular area on the GRAM.

(9) Graphic RAM

The SRAM contained in the graphic RAM can store 172,800-byte bit pattern data by using 18 bits to represent one pixel, which enables displaying at a maximum of 240RGB × 320.

(10) Timing generator circuit

This circuit generates timing signals used to operate the internal circuits necessary for display. The necessary timing for reading GRAM data for display and the timing of internal operations activated by access from a microcomputer are separately controlled, but their mutual interference is prevented. This circuit also generates interface signals (ECS, ESK, EDI, and EDO) to interface with the EEPROM.

(11) Latch circuit (1)

This circuit temporarily stores display data to give preference to GRAM access from the system interface, when an access conflict occurs between the GRAM from the interface and the GRAM to read the data for display. This circuit controls the timing of the display and system interface to prevent mutual interference.

(12) Latch circuit (2)

This is the circuit to temporarily store the digital data of 720 outputs.

(13) Latch circuit (3)

This is a final latch circuit before the digital data of 720 outputs is converted to analog voltage. This circuit serves as an inversion, etc.

(14) Level shifter 1 (LS 1)

This is a voltage step-up circuit that steps the voltage up to liquid crystal drive power supply level to convert the digital data of 720 outputs to analog voltage.

(15) Gradation selection decoder circuit (DEC)

This is a digital-analog converter that converts the digital data of 720 outputs, which has been stepped up to liquid crystal drive power supply level, to a V0 – V63 liquid crystal drive voltage.

(16) Source driving circuit (AMP)

This is an operational amplifier that amplifies the current and outputs a liquid crystal drive voltage of 720 outputs, which has been converted by the gradation selection decoder circuit.

(17) γ-control circuit

This circuit performs gradient-adjustment, fine-adjustment, and amplitude-adjustment of gradation voltage determined at the control register.

(18) Gradation voltage generator circuit

This circuit generates a liquid crystal drive voltage corresponding to the gradation voltage level that is set in the γ-control circuit to make 262,144 colors simultaneously available for display. See "γ adjustment register" for details.

(19) Reference voltage generator circuit

This circuit generates the reference voltage for the regulator circuit.

(20) Regulator

This regulator generates the internal logic power supply VDD.

(21) Liquid crystal driving voltage generating circuit

This circuit generates voltages required for liquid crystal driving (DDVDH, VGH, VGL, and VCL) on the basis of REFVcc.

See the "Instructions" section for the internal DCCLK frequency adjustment for step-up operation and the operation/stop control of the step-up circuit.

The voltage generated here is used for generating Vcom and VREG1OUT.

See the "Instructions" section for the output control.

(22) Scan data generation circuit

The timing generator circuit selects the gate-line output consecutively.

See the "Instructions" section for the number of output lines, scan direction and so on.

(23) Level shifter 2 (LS 2)

VDD – GND, the power supply for the logic circuit, is converted to VGH – VGL, the power supply for the gate driving circuit.

(24) Gate driving circuit

This circuit selects and outputs either VGH or VGL in accordance with a selecting signal generated by the scan data generation circuit and the level shifter. See the "Instructions" section for the number of output lines, scan direction and so on.

GRAM Address Map (BD663474)

Table: Relation between GRAM address and position on display (SS="0", BGR = "0")

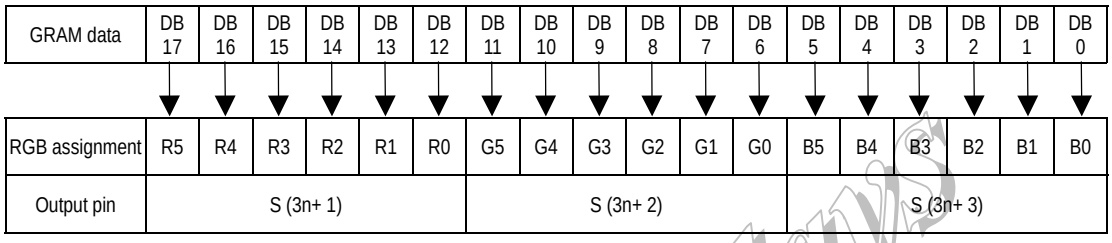
G pins \ S pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB 17	⋯	DB 0	DB 17	⋯	DB 0	DB 17	⋯	DB 0	DB 17	⋯	DB 0	.....	DB 17	⋯	DB 0	DB 17	⋯	DB 0	DB 17	⋯	DB 0	DB 17	⋯	DB 0
G1	G320	"00000"H			"00001"H			"00002"H			"00003"H			.....	"000EC"H			"000ED"H			"000EE"H			"000EF"H		
G2	G319	"00100"H			"00101"H			"00102"H			"00103"H			.....	"001EC"H			"001ED"H			"001EE"H			"001EF"H		
G3	G318	"00200"H			"00201"H			"00202"H			"00203"H			.....	"002EC"H			"002ED"H			"002EE"H			"002EF"H		
G4	G317	"00300"H			"00301"H			"00302"H			"00303"H			.....	"003EC"H			"003ED"H			"003EE"H			"003EF"H		
G5	G316	"00400"H			"00401"H			"00402"H			"00403"H			.....	"004EC"H			"004ED"H			"004EE"H			"004EF"H		
⋮	⋮	⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G316	G5	"13B00"H			"13B01H			"13B02"H			"13B03"H			.....	"13BEC"H			"13BED"H			"13BEE"H			"13BEF"H		
G317	G4	"13C00"H			"13C01"H			"13C02"H			"13C03"H			.....	"13CEC"H			"13CED"H			"13CEE"H			"13CEF"H		
G318	G3	"13D00"H			"13D01"H			"13D02"H			"13D03"H			.....	"13DEC"H			"13DED"H			"13DEE"H			"13DEF"H		
G319	G2	"13E00"H			"13E01"H			"13E02"H			"13E03"H			.....	"13EEC"H			"13EED"H			"13EEE"H			"13EEF"H		
G320	G1	"13F00"H			"13F01"H			"13F02"H			"13F03"H			.....	"13FEC"H			"13FED"H			"13FEE"H			"13FEF"H		

Relation between GRAM address and position on display (SS="1", BGR = "1")

G pins \ S pins		S720	S719	S718	S717	S716	S715	S714	S713	S712	S711	S710	S709	.....	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
GS=0	GS=1	DB 17	⋯	DB 0	DB 17	⋯	DB 0	DB 17	⋯	DB 0	DB 17	⋯	DB 0	.....	DB 17	⋯	DB 0	DB 17	⋯	DB 0	DB 17	⋯	DB 0	DB 17	⋯	DB 0
G1	G320	"00000"H			"00001"H			"00002"H			"00003"H			.....	"000EC"H			"000ED"H			"000EE"H			"000EF"H		
G2	G319	"00100"H			"00101"H			"00102"H			"00103"H			.....	"001EC"H			"001ED"H			"001EE"H			"001EF"H		
G3	G318	"00200"H			"00201"H			"00202"H			"00203"H			.....	"002EC"H			"002ED"H			"002EE"H			"002EF"H		
G4	G317	"00300"H			"00301"H			"00302"H			"00303"H			.....	"003EC"H			"003ED"H			"003EE"H			"003EF"H		
G5	G316	"00400"H			"00401"H			"00402"H			"00403"H			.....	"004EC"H			"004ED"H			"004EE"H			"004EF"H		
⋮	⋮	⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G316	G5	"13B00"H			"13B01H			"13B02"H			"13B03"H			.....	"13BEC"H			"13BED"H			"13BEE"H			"13BEF"H		
G317	G4	"13C00"H			"13C01"H			"13C02"H			"13C03"H			.....	"13CEC"H			"13CED"H			"13CEE"H			"13CEF"H		
G318	G3	"13D00"H			"13D01"H			"13D02"H			"13D03"H			.....	"13DEC"H			"13DED"H			"13DEE"H			"13DEF"H		
G319	G2	"13E00"H			"13E01"H			"13E02"H			"13E03"H			.....	"13EEC"H			"13EED"H			"13EEE"H			"13EEF"H		
G320	G1	"13F00"H			"13F01"H			"13F02"H			"13F03"H			.....	"13FEC"H			"13FED"H			"13FEE"H			"13FEF"H		

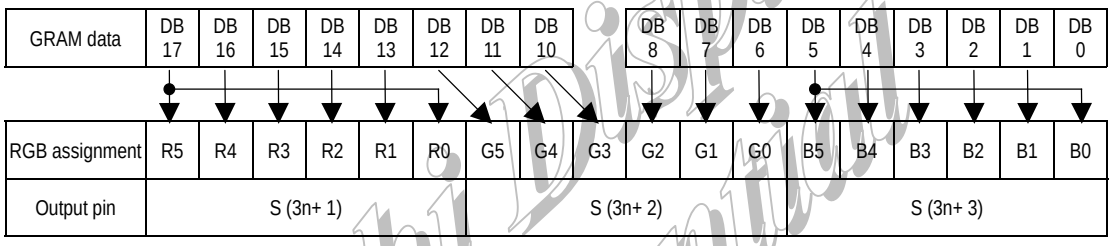
Relation between GRAM data and display data (SS="0", BGR="0")
The following diagram illustrates the relationship between data to be written to the GRAM and display data in each interface mode.

■ **80-series 18-bit interface (1 transfer/pixel)**



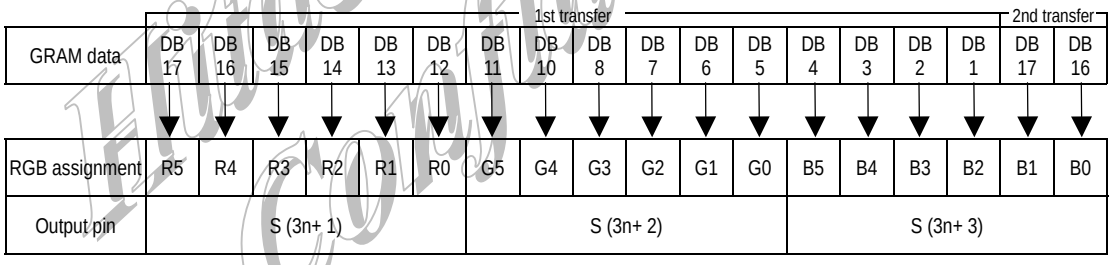
Note1) n = Lower 8 bits of address (0~239)
Note2) 262,144-color display available

■ **80-series 16-bit interface (1 transfer/pixel)**



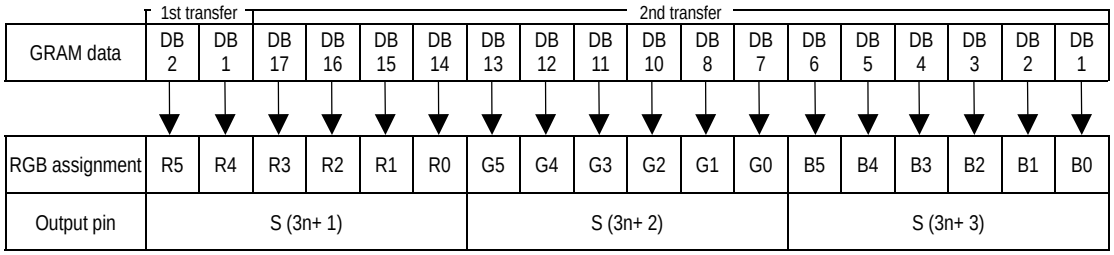
Note1) n = Lower 8 bits of address (0~239)
Note2) 65,536color display available

■ **80-series 16-bit interface (2 transfers/pixel) 1**



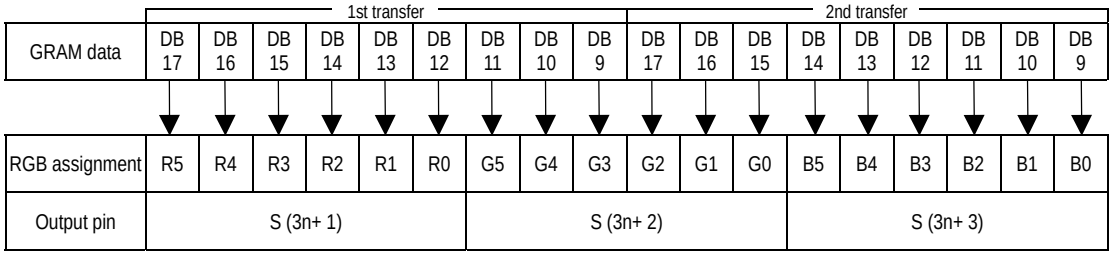
Note1) n = Lower 8 bits of address (0~239)
Note2) 262,144-color display available

■ **80-series 16-bit interface (2 transfers/pixel) 2**



Note1) n = Lower 8 bits of address (0~239)
Note2) 262,144-color display available

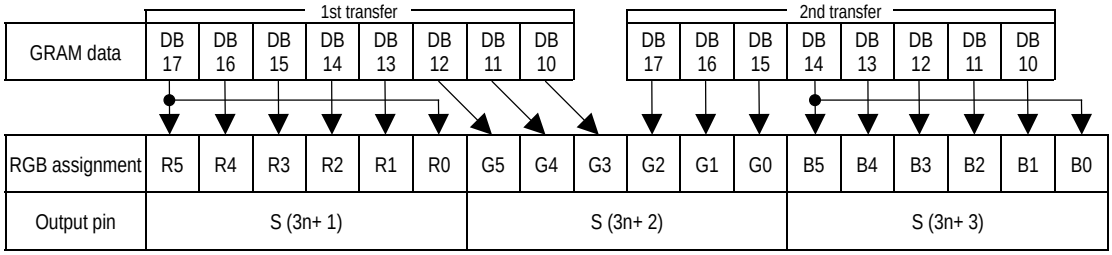
■ **80-series 9-bit interface (2 transfers/pixel)**



Note1) n = Lower 8 bits of address (0~239)

Note2) 262,144-color display available

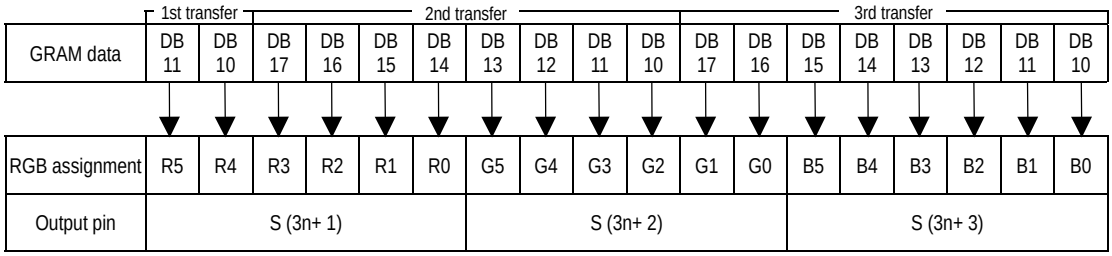
■ **80-series 8-bit interface (big-endian) / SPI (2 transfers/pixel**



Note1) n = Lower 8 bits of address (0~239)

Note2) 65,536color display available

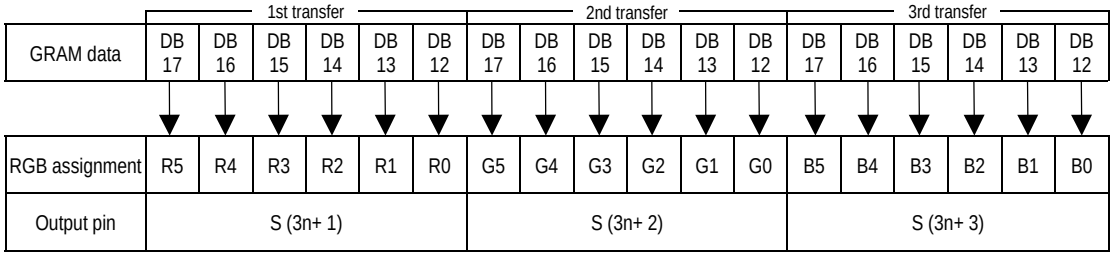
■ **80-series 8-bit interface (3 transfers/pixel) 1**



Note1) n = Lower 8 bits of address (0~239)

Note2) 262,144-color display available

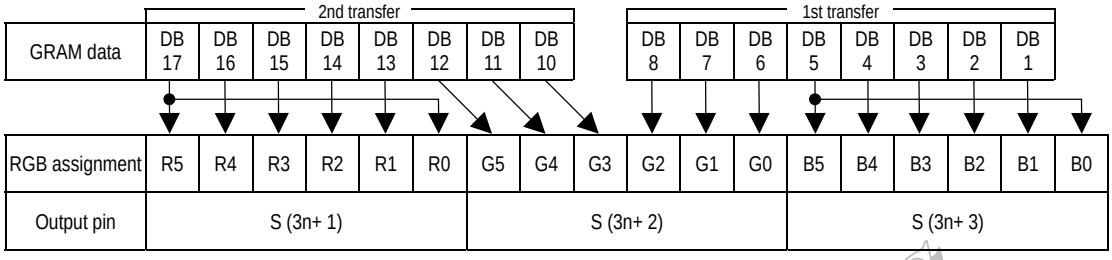
■ **80-series 8-bit interface (3 transfers/pixel) 2**



Note1) n = Lower 8 bits of address (0~239)

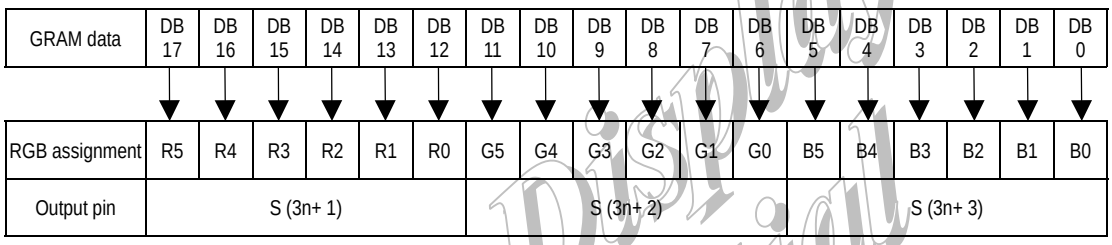
Note2) 262,144-color display available

■ **80-series 8-bit interface (little-endian) (2 transfers/pixel)**



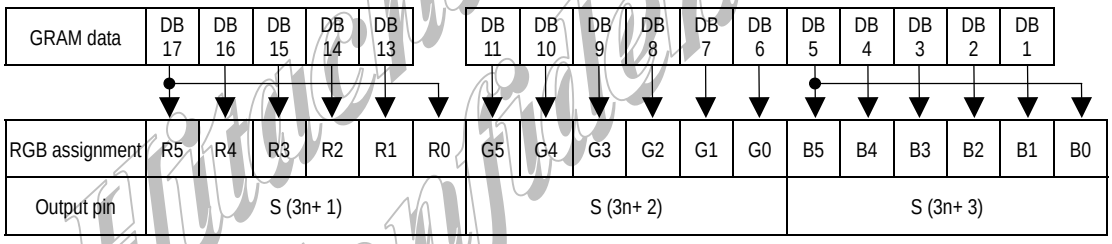
Note1) n = Lower 8 bits of address (0~239)
Note2) 65,536color display available

■ **18-bit RGB interface (1 transfer/pixel)**



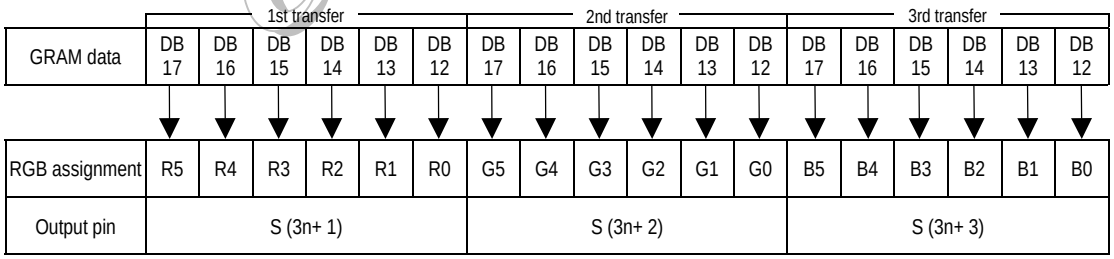
Note1) n = Lower 8 bits of address (0~239)
Note2) 262,144-color display available

■ **16-bit RGB interface (1 transfer/pixel)**



Note1) n = Lower 8 bits of address (0~239)
Note2) 65,536color display available

■ **6-bit RGB interface (3 transfers/pixel)**

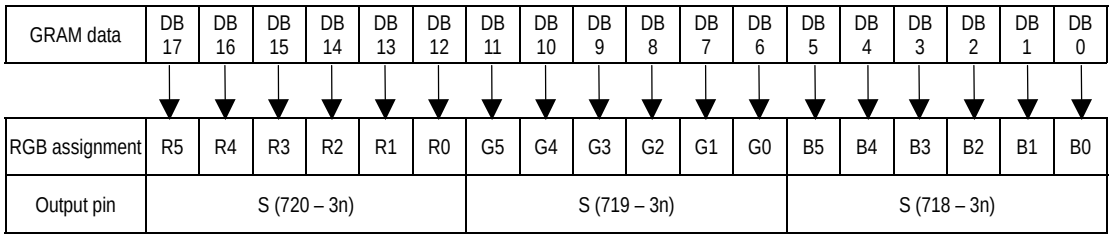


Note1) n = Lower 8 bits of address (0~239)
Note2) 262,144-color display available

Relation between GRAM data and display data (SS="1", BGR="1")

The following diagram illustrates the relationship between data to be written to the GRAM and display data in each interface mode.

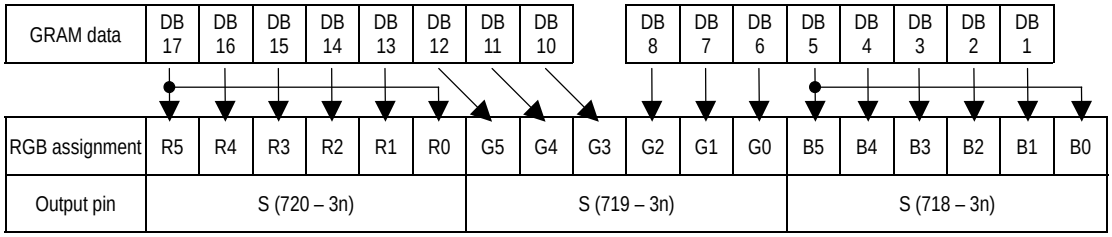
■ **80-series 18-bit interface (1 transfer/pixel)**



Note1) n = Lower 8 bits of address (0~239)

Note2) 262,144-color display available

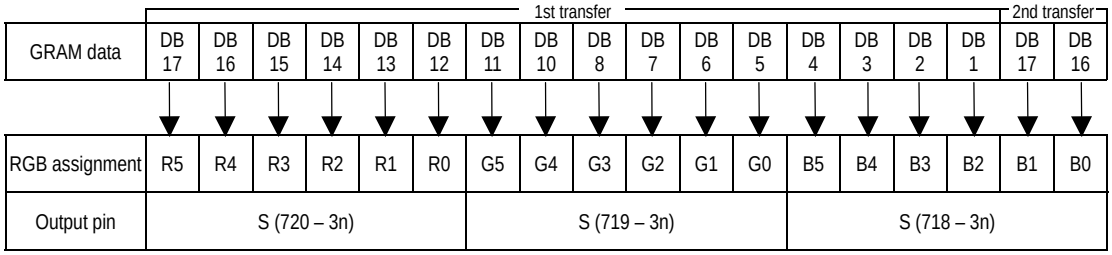
■ **80-series 16-bit interface (1 transfer/pixel)**



Note1) n = Lower 8 bits of address (0~239)

Note2) 65,536color display available

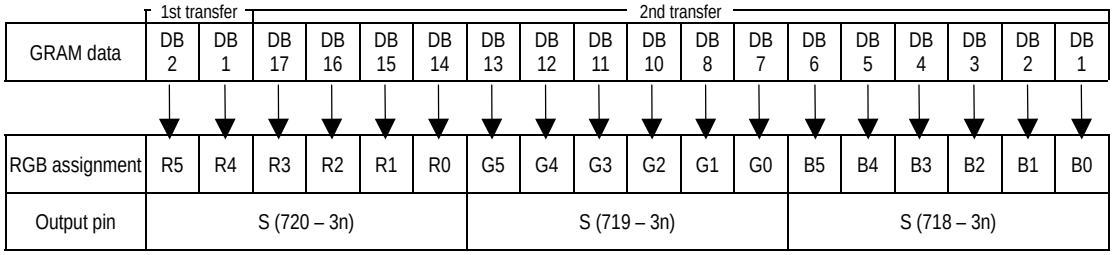
■ **80-series 16-bit interface (2 transfers/pixel) 1**



Note1) n = Lower 8 bits of address (0~239)

Note2) 262,144-color display available

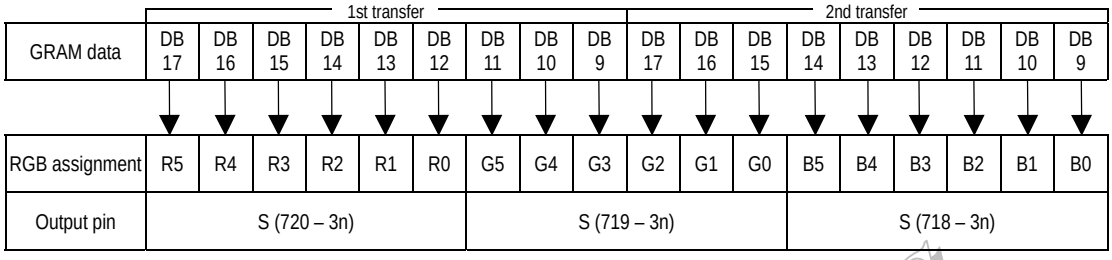
■ **80-series 16-bit interface (2 transfers/pixel) 2**



Note1) n = Lower 8 bits of address (0~239)

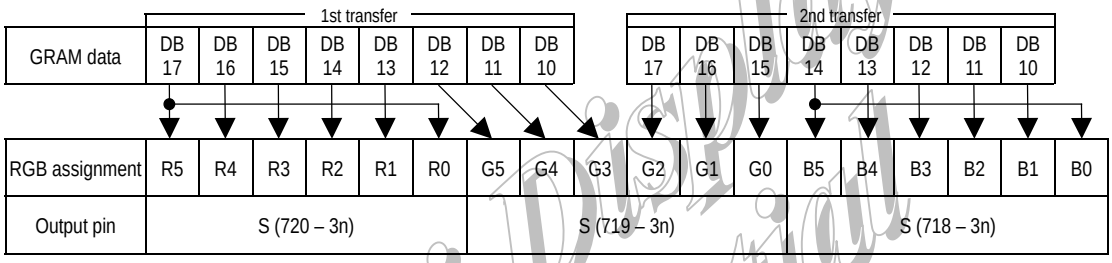
Note2) 262,144-color display available

■ **80-series 9-bit interface (2 transfers/pixel) 1**



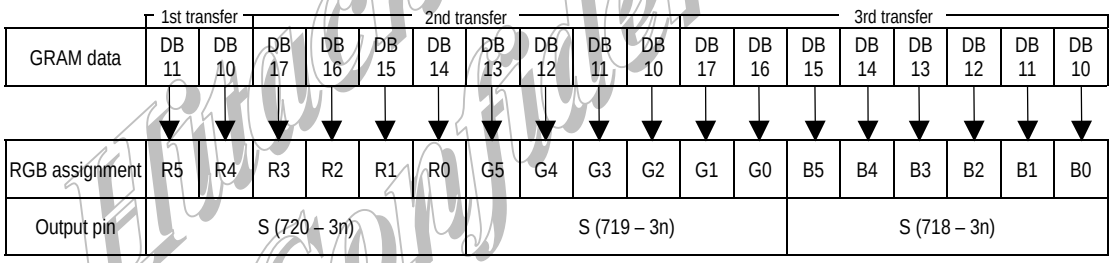
Note1) n = Lower 8 bits of address (0~239)
Note2) 262,144-color display available

■ **80-series 8-bit interface (big-endian) / SPI (2 transfers/pixel)**



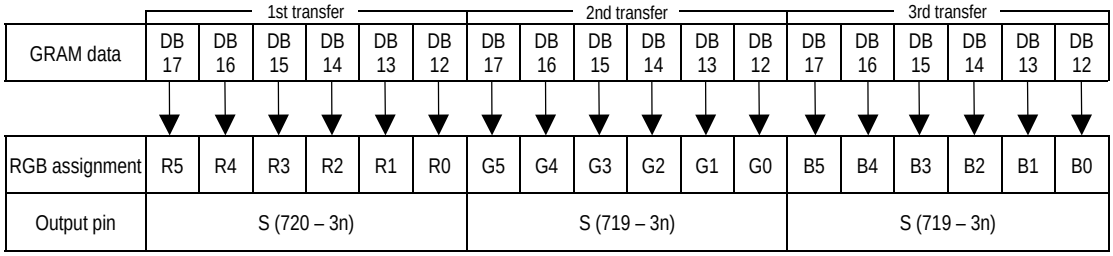
Note1) n = Lower 8 bits of address (0~239)
Note2) 65,536color display available

■ **80-series 8-bit interface (3 transfers/pixel) 1**



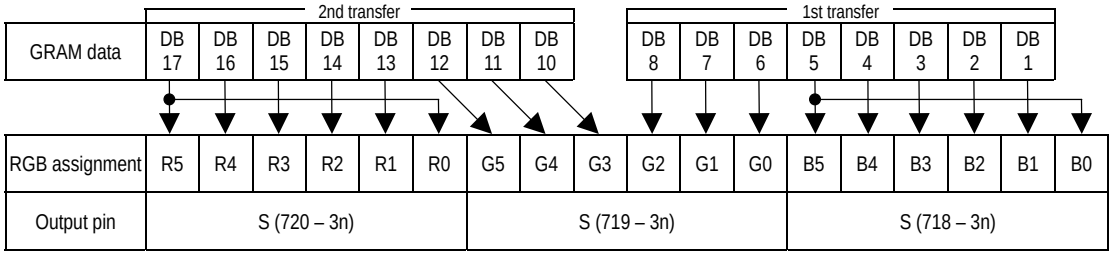
Note1) n = Lower 8 bits of address (0~239)
Note2) 262,144-color display available

■ **80-series 8-bit interface (3 transfers/pixel) 2**



Note1) n = Lower 8 bits of address (0~239)
Note2) 262,144-color display available

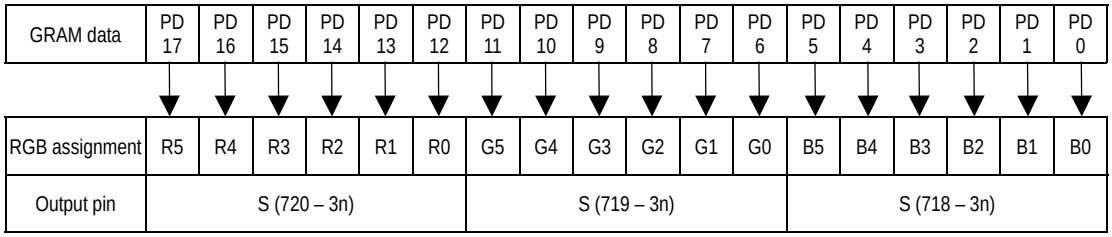
■ **80-series 8-bit interface (little-endian) (2 transfers/pixel)**



Note1) n = Lower 8 bits of address (0~239)

Note2) 65,536color display available

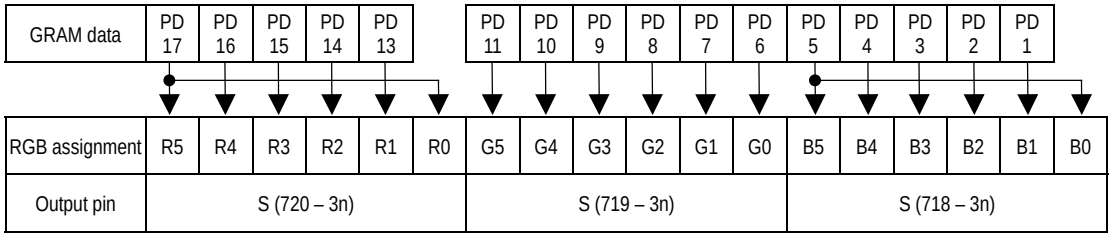
■ **18-bit RGB interface (1 transfer/pixel)**



Note1) n = Lower 8 bits of address (0~239)

Note2) 262,144-color display available

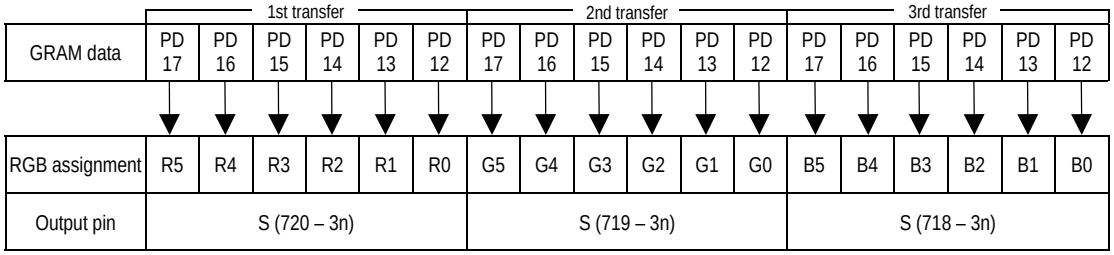
■ **16-bit RGB interface (1 transfer/pixel)**



Note1) n = Lower 8 bits of address (0~239)

Note2) 65,536color display available

■ **6-bit RGB interface (3 transfers/pixel)**



Note1) n = Lower 8 bits of address (0~239)

Note2) 262,144-color display available

Instructions

- **Overview**

The BD663474 employs an 18-bit bus architecture to enable a high-speed interface with high-performance microcomputers.

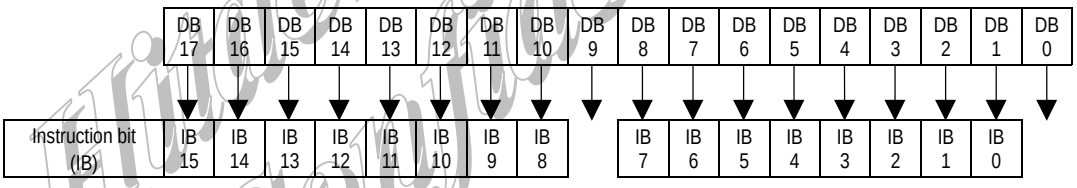
Externally sent 18/16/9/8-bit data is stored in the instruction register and used to start up internal operations. Since the signals from microcomputers decide internal operations, they are called instructions including the register select signal (RS), write strobe signal (WR*), read strobe signal (RD*), and internal 16-bit data bus signals (IB15 to IB0). Internal 18-bit is used when accessing the internal RAM. Instructions are grouped into the following types:

(1) Index specifying instructions
(2) Status read instructions
(3) Instructions for display control
(4) Instructions for power management control
(5) Instructions for graphic data processing
(6) Instructions for internal RAM access control
(7) Instructions for internal adjustment of γ properties

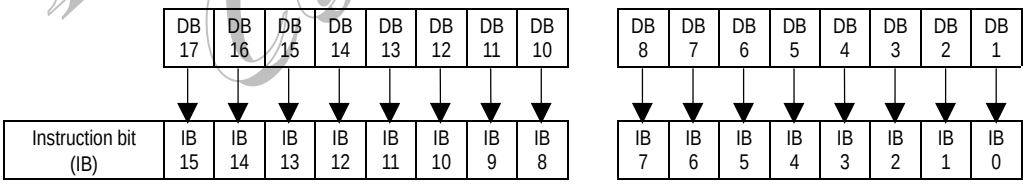
The address on the internal RAM is automatically updated after data is written. This feature, combined with the window address function, minimizes the data transfer volume and therefore reduces the program load of the microcomputer. Instructions are executed with a 0 cycle, enabling continuous writing.

Refer to the "System Interfaces" section for the pin assignment to the instruction bits (IB15 – 0) for each interface. Instructions must adopt the data format of the interface in use.

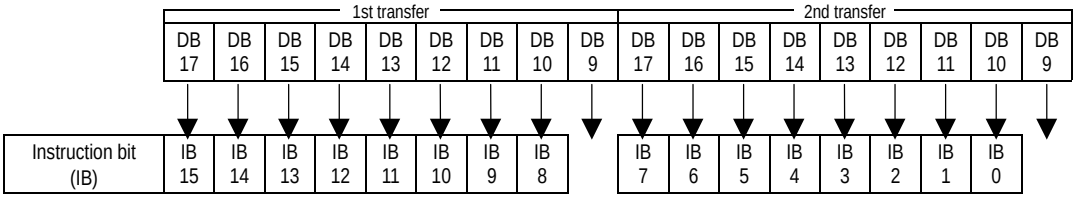
■ **80-series 18-bit interface (1 transfer)**



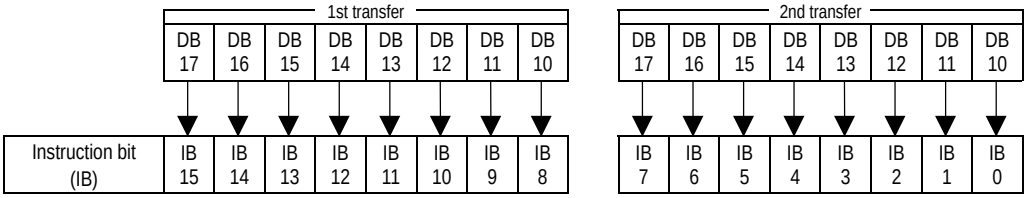
■ **80-series 16-bit interface (1 transfer)**



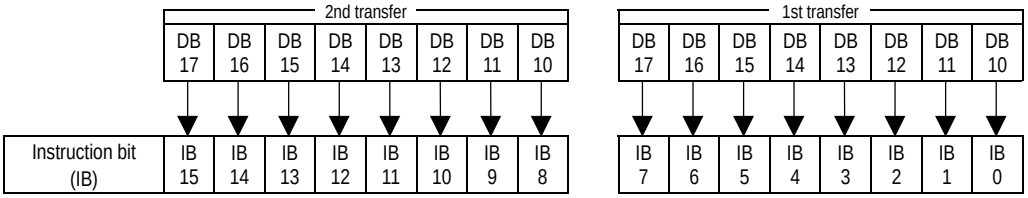
■ **80-series 9-bit interface (2 transfers)**



■ **80-series 8-bit interface (big-endian) / SPI interface (2 transfers)**

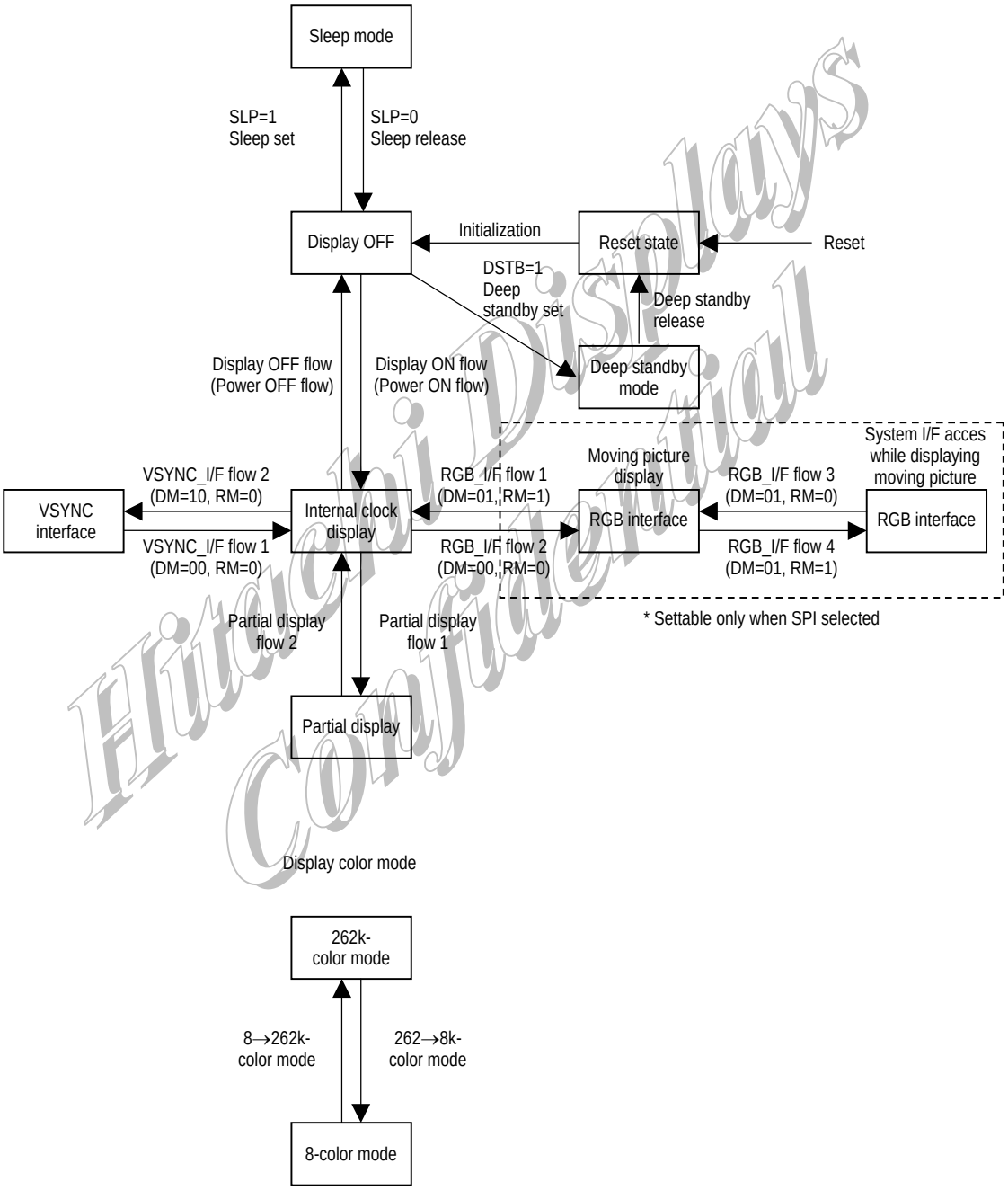


■ **80-series 8-bit interface (little-endian) (2 transfers)**



Basic Operation Modes

The following diagram illustrates the basic operation modes of the BD663474.
Refer to “Instruction Setup Flow” for the transition from each operation mode.



Detailed description

Note that instruction details are described as follows by using the instruction bits (IB15 – 0) assigned to the respective interfaces.

■ **Index/status/display control instructions**

(1) Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index of the control register or GRAM control to be accessed using an 11-bit binary number. Access to the instruction bit is prohibited unless the index is not assigned.

(2) Status Read (SR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	0	0	0	0	0	0	0	L8	L7	L6	L5	L4	L3	L2	L1	L0

The status read reads the internal status of the BD663474.
L8-0: Indicates the line where liquid crystal is currently driven.

(3) Start Oscillation (R000h)

Device Code Read

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	1	1	0	1	0	0	0	1	1	1	0	1	0	0

"3474"H is read out when reading out this register forcibly.

(4) Driver Output Control (R001h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SS	0	0	0	0	0	0	0	0

SS Defines the relation between the source driver output and GRAM address.
Refer to "GRAM address map" for details.

Select the SS bit and BGR bit when changing the dot arrangements of (R), (G) and (B).
When SS = 0 and BGR = 0, addresses are assigned to (R), (G) and (B) from the S1 pin.
When SS = 1 and BGR = 1, addresses are assigned to (R), (G) and (B) from the S720 pin.
When changing the SS and BGR bits, GRAM data must be rewritten.

(5) LCD Driver Wave Control (R002h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	NW1	NW0

B/C When B/C = 0, a frame inversion drive is selected. Alternating timing is turned on for each screen to drive the liquid crystal.
When B/C = 1, an n- line inversion drive is selected. Alternating timing is turned on for every n line as specified with NW1-0 bits of the liquid crystal alternating driving control register. Refer to "n-line inversion liquid crystal drive" for details.

NW1–0 When a C pattern waveform is selected (B/C = 1), it specifies "n", the number of lines to inverse. Lines from 1 to 4 are selectable as the inversion occurs every n + 1 line.

(6) Entry Mode 1 (R003h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D [1]	I/D [0]	AM	0	0	0

AM This sets the direction of automatically updating the address counter (AC) after data is written to the GRAM.
When AM = 0, writes continuously in the horizontal direction.
When AM = 1, writes continuously in the vertical direction.
When making a window address area, data is written to the GRAM area specified by window addresses in the manner set with I/D and AM.

I/D [1:0] This sets the automatic increment (+1) or decrement (–1) of the address counter (AC) after data is written to the GRAM. I/D [0] sets the increment or decrement of the lower addresses (AD7-0) in the horizontal direction. I/D [1] sets the increment or decrement of the upper addresses (AD16-8) in the vertical direction. The AM bit specifies the transition direction of the address after writing data to the GRAM.

ORG When ORG = 1, the start position designated in setting the window address area is shifted in accordance with the I/D bit setting.
Set ORG =0 during RAM read operation.

HWM When HWM = 1, data is written to the GRAM at high speed. In high-speed write mode, one line of data is buffered before being written to the GRAM.
When HWM = 1, make sure that AM = 0 (horizontal direction) and a data write operation is executed for each line of the window address area. Data will not be written properly in a line where writing is terminated in the middle. Refer to “High-speed RAM write mode” for details.

BGR Reverses the order of dots from RGB to BGR for the 18-bit data to be written to the GRAM.

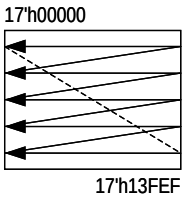
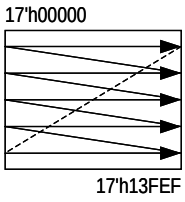
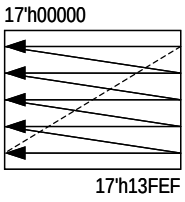
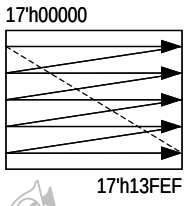
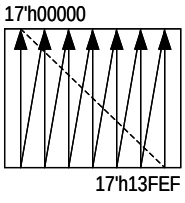
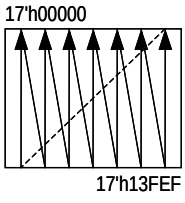
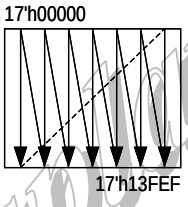
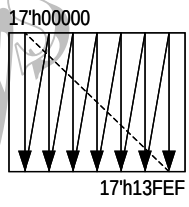
DFM When IM3-0 = (GND, GND, VccIO, VccIO), sets the data format for three-time transfer RAM writing in conjunction with the TRI bit through the 80-series 8-bit bus interface.
DFM = 0: RGB 18-bit data is written in three byte-boundary transfers.
DFM = 1: RGB 18-bit data is written in three 6-bit transfers.

When IM3-0 = (GND, GND, VccIO, GND), sets the data format for two-time transfer RAM writing in conjunction with the TRI bit through the 80-series 16-bit bus interface.
DFM = 0: RGB 18-bit data is written in two MSB-format transfers.
DFM = 1: RGB 18-bit data is written in two LSB-format transfers.

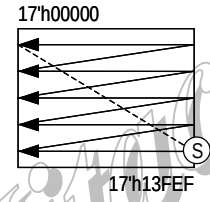
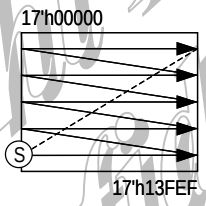
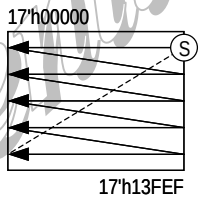
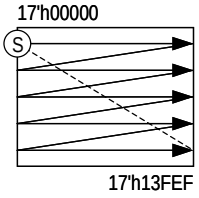
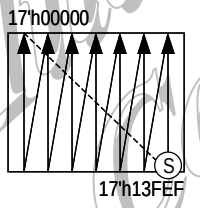
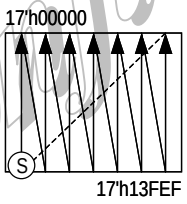
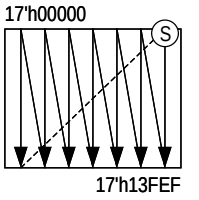
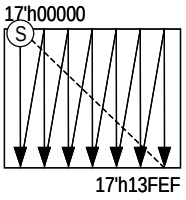
Always set DFM = 0 when not using an 8-bit or 16-bit interface.

TRI When IM3-0 = (GND, GND, VccIO, VccIO), sets the number of data transfers to the RAM (2 transfers / 3 transfers) through the 80-series 8-bit bus interface.
TRI = 0: 16-bit RAM data is transferred in two transfers.
TRI = 1: 18-bit RAM data is transferred in three transfers.

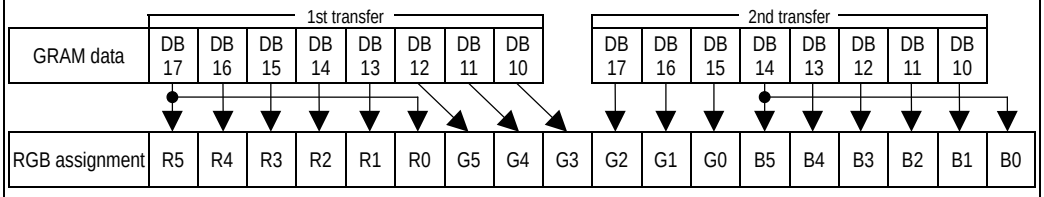
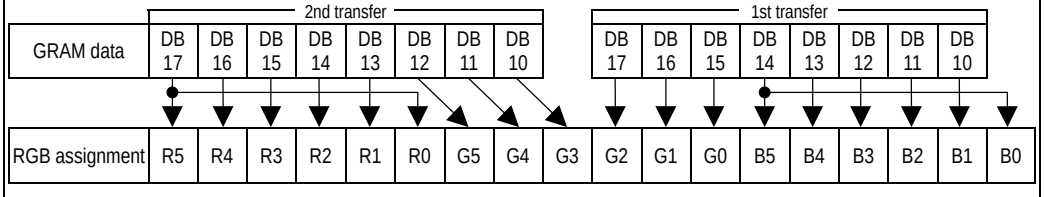
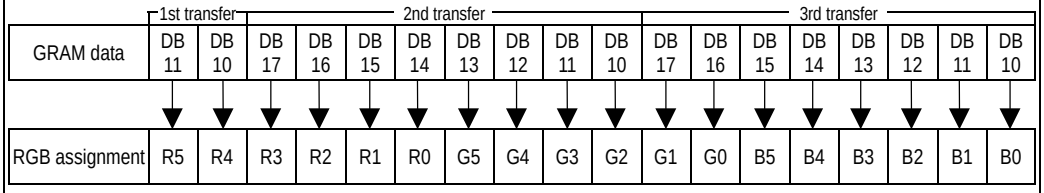
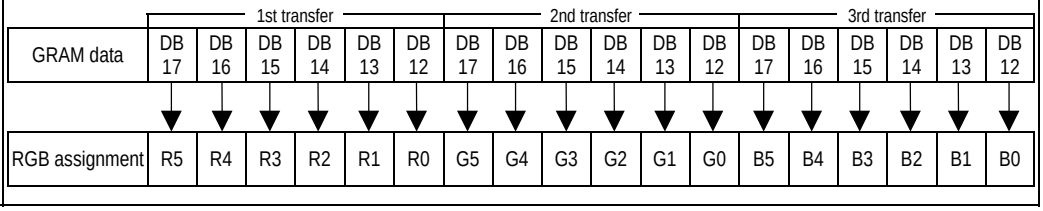
When IM3-0 = (GND, GND, VccIO, GND), set the number of data transfers to the RAM (1 transfer or 2 transfers) through the 80-series 16-bit but interface.
TRI = 0: 16-bit RAM data is transferred in one transfer.
TRI = 1: 18-bit RAM data is transferred in two transfers.
TRI must be set to 0 when not using an 8-bit or 16-bit interface. During GRAM read operation, also set TRI=0.

ORG=0	I/D[1:0] = "00" H-direction: Decrement V-direction: Decrement	I/D[1:0] = "01" H-direction: Increment V-direction: Decrement	I/D[1:0] = "10" H-direction: Decrement V-direction: Increment	I/D[1:0] = "11" H-direction: Increment V-direction: Increment
AM = "0" Horizontal direction				
AM = "1" Vertical direction				

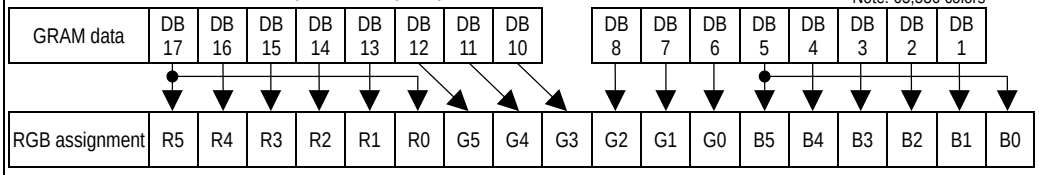
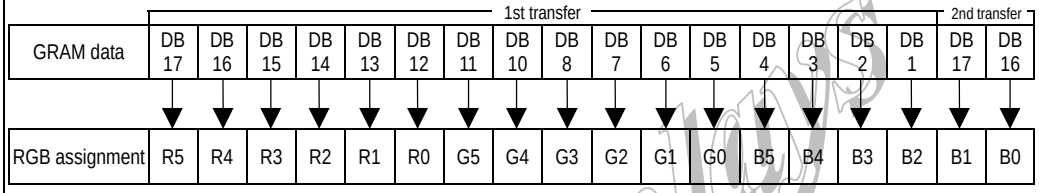
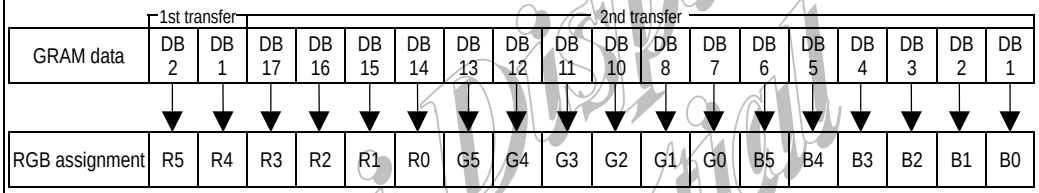
Note: Writing is available only to the GRAM within the window address when setting the window address.

ORG=1	I/D[1:0] = "00" H-direction: Decrement V-direction: Decrement	I/D[1:0] = "01" H-direction: Increment V-direction: Decrement	I/D[1:0] = "10" H-direction: Decrement V-direction: Increment	I/D[1:0] = "11" H-direction: Increment V-direction: Increment
AM = "0" Horizontal direction				
AM = "1" Vertical direction				

Note: When ORG = 1, writing to the RAM starts from the address at the corner (S) in the area.

TRI	DFM	8-bit interface RAM write transfer formula (IM3–0 =(GND, GND, Vcc, VccIO))
0	*	■ 80-series 8-bit interface (big-endian) (2 transfers/pixel) Note: 65,536 colors 
0	*	■ 80-series 8-bit interface (little-endian) (2 transfers/pixel) Note: 65,536 colors 
1	0	■ 80-series 8-bit interface (3 transfers/pixel) 1 Note: 262,144 colors 
1	1	■ 80-series 8-bit interface (3 transfers/pixel) 2 Note: 262,144 colors 

Note: Instructions in 8-bit interface mode (IM3-0 = (GND, GND, VccIO, VccIO) are transferred in two 8-bit transfers regardless of TRI and DFM settings.

TRI	DFM	16-bit interface RAM write transfer formula (IM3–0 =(GND, GND, VccIO, GND))
0	*	■ 80-series 16-bit interface (1 transfer/pixel) Note: 65,536 colors 
1	0	■ 80-series 16-bit interface (2 transfers/pixel) 1 Note: 262,144 colors 
1	1	■ 80-series 8-bit interface (2 transfers/pixel) 2 Note: 262,144 colors 

Note: Instructions in 16-bit interface mode (IM3-0 = (GND, GND, VccIO, GND) are transferred in one 16-bit transfer regardless of TRI and DFM settings.

(7) Resizing Control (R004h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	RCV [1]	RCV [0]	0	0	RCH [1]	RCH [0]	0	0	RSR [1]	RSR [0]

RSR [1:0] This sets the contraction rate applied when writing data to GRAM. Data is written to the GRAM according to this contraction rate in horizontal and vertical directions. Refer to “Resizing function” for details.

RCH [1:0] This sets the horizontal pixel surplus which is created when resizing (contracting) a picture. By specifying the number of surplus pixels with the RCH bits, it is possible to transfer data regardless of the number of surplus pixels. Only set when using the resizing function. Make sure that RCH = 2’h0 when the resizing function is not used (RSR = 2’h0).

RCV [1:0] This sets the vertical pixel surplus which is created when resizing (contracting) a picture. By specifying the number of surplus pixels with the RCV bits, it is possible to transfer data regardless of the number of surplus pixels. Only set when using the resizing function. Make sure that RCV = 2’h0 when the resizing function is not used (RSR = 2’h0).

■ **Resizing (contraction) rate setting (RSR)**

RSR [1 : 0]	Resizing rate
2'h0	No resizing (× 1)
2'h1	× 1/2
2'h2	Setting disabled
2'h3	× 1/4

■ **Horizontal pixel surplus (RCH)**

RCH [1 : 0]	Resizing rate
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixel
2'h3	3 pixel

■ **Vertical pixel surplus (RCV)**

RCV [1 : 0]	Resizing rate
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixel
2'h3	3 pixel

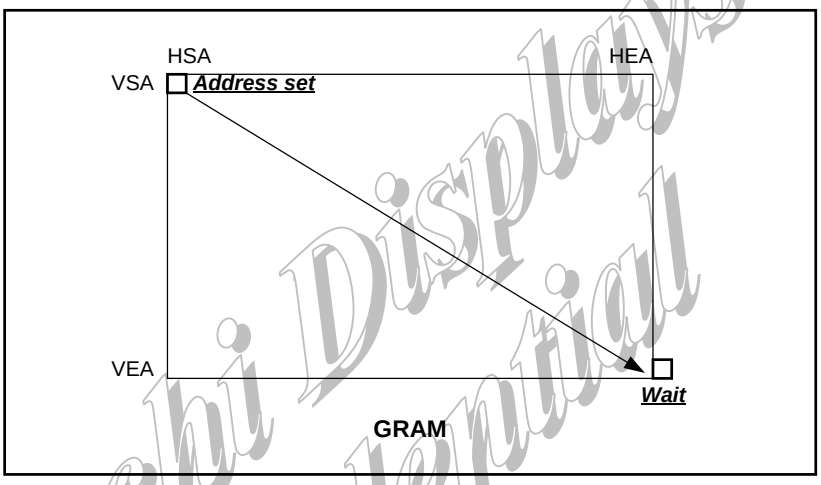
Note: 1 pixel = 1 RGB

(8) Moving Picture Control (006h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	COE [4]	COE [3]	0	COE [2]	COE [1]	COE [0]	0	0	EEE [1]	EEE [0]

EEE [1:0] This is a register to improve the sharpness of moving pictures. This function is effective when EEE [1:0] = 2'b11.

COE [4:0] This is a register to adjust the degree of image processing.



Note 1: The RAM address must be set (R200h/R201h) at the start of the window in accordance with the entry mode.

Note 2: One wait (normally two RAM write cycles) is required for every RAM writing (HEA-HAS + 1) × (VEA-VSA + 1) of one frame.

(9) Display Control 1 (R007h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	PTDE [1]	PTDE [0]	0	0	0	BASEE	0	0	0	DTE	0	0	D [1]	D [0]

D [1:0] D[1] = 1 starts graphic display, and D[1] = 0 turns all the displays off. As the display data is retained in the GRAM, setting D[1] = 1 restarts displaying instantly.
When the display is turned off by setting D[1] = 0, all source outputs become GND level to reduce the charging/discharging current on liquid crystal cells which is generated during liquid crystal inversion drive.
D[1:0] = 2'h1 turns off the display, and all internal display operation of the BD663474 is lost.
D[1:0] = 2'h0 stops the internal display operation and turns off the display. In combination with GON and DTE, it controls the on/off of the display. Refer to "Instruction Setup Flow" for details.

D[1:0]	Source output	BD663474 Internal operation	BLDsignal
2'h0	GND	Stop	Stop
2'h1	GND	Run	Run
2'h2	Non-display	Run	Run
2'h3	display	Run	Run

Note 1: The write operation of data from a microcomputer is not affected by the D[1:0] setting.
Note 2: D[1:0] = 2'h0 in standby mode. This does not mean the register content of D[1:0] is changed.
Note 3: Source output with non-display must be in accordance with the PTS[2:0] bit setting.

DTE This controls the gate output in combination with the GON.

DTE	GON	Gate output
0	0	VGH
	1	VGL
1	0	VGH
	1	VGH / VGL (normal operation)

BASEE Enable bit for base image display. The BASEE setting is effective when D[1:0] = 2'h3. With any setting other than D[1:0] = 2'h3, the source output is in accordance with the D[1:0] bit setting.

BASEE	Source output
0	Non-display or partial display
1	Base image display

Note 1: Source output with non-display must be in accordance with the PTS bit setting.
Note 2: Gate scan with non-display must be in accordance with the PTG setting.

PTDE[1:0] Enables bit for partial display. The BASEE setting is effective when D[1:0] = 2'h3. With any setting other than D[1:0] = 2'h3, the source output is in accordance with the D[1:0] bit setting.

PTDE[1] / PTDE[0]	Source output
0	Non-display or partial display
1	Partial display

Note 3: Set BASEE = 0 when PTDE[1] = 1 or PTDE[0] = 1.

(10) Display Control 2 (R008h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP [3]	FP [2]	FP [1]	FP [0]	0	0	0	0	BP [3]	BP [2]	BP [1]	BP [0]

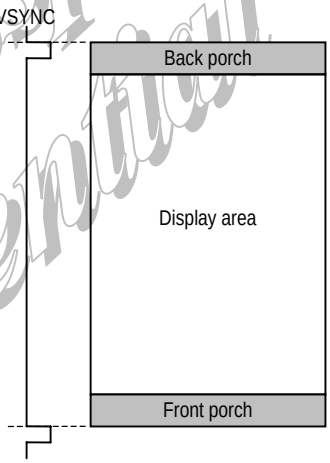
FP [3:0] This sets the duration of the blank period (front/back porches) to be provided at the beginning and end of the display.

BP [3:0] FP[3:0] specifies the number of front porch lines and BP[3:0] specifies the number of back porch lines.

BP + FP ≤ 16 lines
BP ≥ 2lines
FP ≥ 2lines

In external display interface mode, a back porch (BP) starts on the falling edge of VSYNC, followed by display operation. After driving the number of lines set by the NL bit, a front porch (FP) starts. After the front porch, a blank period continues until the next input of the VSYNC signal.

FP[3:0] BP[3:0]	Number of front porch lines Number of back porch lines
4'h0	Setting disabled
4'h1	Setting disabled
4'h2	2 lines
4'h3	3 lines
4'h4	4 lines
⋮	⋮
4'hC	12 lines
4'hD	13 lines
4'hE	14 lines
4'hF	Setting disabled



(11) Display Control 3 (R009h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PTS [2]	PTS [1]	PTS [0]	0	0	PTG [1]	PTG [0]	0	0	ISC [1]	ISC [0]

ISC [1:0] This sets the scan cycle by the gate driver when the PTG bits are set to the interval scan in the non-display area. The scan cycle is set at n frames, where n is an odd number. The polarity is inverted as the scan is executed.

ISC[1:0]	Scan cycle
3'h0	Every frame
3'h1	3 frames
3'h2	5 frames
3'h3	7 frames

PTG [1:0] Set the DISPTMG signal to determine the scan mode by the gate driver in the non-display area.

PTG[1:0]	Gate output in non-display area	Source output in display area
2'h0	Normal scan	According to PTS setting
2'h1	VGL (fixed)	According to PTS setting
2'h2	Interval scan	According to PTS setting
2'h3	–	–

Note: Set the frame inversion drive when using an interval scan.

PTS [1:0] This sets the source output in non-display driving. This setting is applied to front/back porch periods and all non-display areas. It is also applied to front/back porch periods and non-display areas of partial display. When PTS[2] = 1, the gradation amplifier is stopped except for V0 and V63 during non-display driving in order to reduce power consumption.

PTS[2:0]	Non-display source output		Step-up clock frequency in non-display area
	Positive polarity	Negative polarity	
3'h0	V63	V0	According to DC0 and DC1 settings
3'h1	Setting disabled	Setting disabled	–
3'h2	GND	GND	According to DC0 and DC1 settings
3'h3	Hi-Z	Hi-Z	According to DC0 and DC1 settings
3'h4	V63	V0	1/2 the frequency of DC0 and DC1 settings
3'h5	Setting disabled	Setting disabled	–
3'h6	GND	GND	1/2 the frequency of DC0 and DC1 settings
3'h7	Hi-Z	Hi-Z	1/2 the frequency of DC0 and DC1 settings

Note 1: Gate output in the non-display area is controlled by the PTG setting.

Note 2: On/Off of the gradation amplifier and slowing down the frequency of step-up clocks are applied only to the non-display area.

Note 3: The frequency of step-up clocks is not halved by setting PTS[2:0] to 3'h4, 3'h6, or 3'h7 while DC[4:3] = 2'h3.

(12) Display Control 5 (R00Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CL	0

CL CL = 1 sets 8-color mode.

Follow the setting sequence described in “8-color display mode”.

CL	Available colors for display
0	262,144 colors
1	8 colors

(13) External Display Interface Control 1 (R00Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM [1]	DM [0]	0	0	RIM [1]	RIM [0]

RIM [1:0] This sets RGB interface mode when selecting the RGB interface with DM and RM bits. Carry out this setting before starting display operation through an external display interface. Do not change the setting during display operation.

RIM[1:0]	RGB interface mode	Available colors
2'h0	18-bit RGB interface (1 transfer/pixel)	262,144 colors
2'h1	16-bit RGB interface (1 transfer/pixel)	65,536 colors
2'h2	6-bit RGB interface (3 transfers/pixel)	262,144 colors
2'h3	Setting disabled	

Note 1: Instruction register setting is available only through the system interface.

Note 2: Make sure that data transfers and DOTCLK inputs are executed in units of RGB dots when using a 6-bit RGB interface.

DM [1:0] This sets the display operation mode and selects the interface through which the display operation is executed. This setting enables switching between internal clock operation mode and external display interface mode. Do not switch between the two external interface modes (RGB I/F and VSYNC I/F).

DM[1:0]	Display operation interface
2'h0	Internal clock operation
2'h1	RGB interface
2'h2	VSYNC interface
2'h3	Setting disabled

Note: You can only set DM = 2'h1 when SPI is selected.

RM This sets the interface to access the GRAM. GRAM access is possible only through an interface that is set with the RM bit. Set RM = 1 when writing display data through the RGB interface. When RM = 0, the display data can be changed through the system interface even while performing the display operation through the RGB interface, since the RM is settable separately from the display operation mode.

RM	Interface to access GRAM
0	System interface / VSYNC interface
1	RGB interface

Note: You can only set RM = 1 when SPI is selected.

RM and DM must be set for each state of display as shown in the following table. Use high-speed write mode (HWM = 1) when displaying a moving picture (RGB interface or VSYNC interface).

State of display	Operation mode	GRAM access setting (RM)	Display operation mode (DM)
Still picture	Internal clock only	System interface (RM = 0)	Internal clock operation (DM = 2'h0)
Moving picture	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM = 2'h1)
Update still picture area during moving picture display	RGB interface (2)	System interface (RM = 0)	RGB interface (DM = 2'h1)
Moving picture	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM = 2'h2)

Note 1: Instructions must be set through the system interface.
Note 2: Switching between the RGB and VSYNC interfaces is not possible.
Note 3: Do not make changes to the RIM setting while the RGB interface is in operation.
Note 4: Refer to "External interfaces" for the operation mode transition.

- Internal clock operation mode

  All display operations are synchronized with internally generated operating clocks in this mode. All inputs through the external display interface are invalid. The GRAM is accessible only through the system interface.

- RGB interface mode (1)

  The display operation is synchronized with the frame synchronizing signal (VSYNC), the line synchronizing signal (HSYNC), and the dot clocks (DOTCLK) in RGB interface mode. These signals must be supplied through the display period using the RGB interface. Display data are transferred in units of pixels through the DB17-0 pins. All display data is stored in the GRAM. The combined use of high-speed RAM write mode and window address function enables the display of data in a moving picture area and data in the GRAM at once, which makes it possible to transfer display data when only rewriting the display data, and contributes to minimizing data transfers.

  The front porch (FP), back porch (BP), and display duration (NL) are generated inside the IC by counting the clocks of the frame synchronizing signal (VSYNC) and the line synchronizing signal (HSYNC). Pixel data must be transferred through the DB17-0 pins in accordance with the above mentioned settings.

- RGB interface mode (2)

  GRAM data can be rewritten through the system interface when RGB interface mode is selected. Make sure that the display data is not being transferred through the RGB interface (ENABLE = HIGH), when rewriting the GRAM. To return to display data transfer mode using the RGB interface, change the setting first as in the above table and then set a new address and the index (R202h).

- VSYNC interface mode

  The internal display operation is synchronized with the frame synchronizing signal (VSYNCC) in VSYNC interface mode. A moving picture can be displayed through the current system interface by writing the display data to the GRAM at a constant speed through a system interface from the falling edge of the frame synchronizing signal (VSYNC). In this case, there are constraints in the GRAM writing speed and methods. Refer to "External display interface" for details.

  Only VSYNC inputs are valid in VSYNC interface mode. Other signal inputs through the external display interface are invalid.

  The front porch (FP), back porch (BP), and display duration (NL) are generated inside the IC by counting the clocks of the frame synchronizing signal (VSYNC).

(14) Frame Cycle Control (R00Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVI [1]	DIVI [0]	0	0	0	RTNI [4]	RTNI [3]	RTNI [2]	RTNI [1]	RTNI [0]

RTNI [4:0] This sets the 1H (1 line) period.

DIVI [1:0] This sets the division ratio of internal clocks (DIVI). The internal operation is performed according to the clocks set by DIVI[1:0]. This can adjust the frame frequency in conjunction with the 1H period (RTNI). The frame frequency is adjusted when changing the number of driven lines. Refer to "Frame frequency adjustment function" for details.
* This function is invalid when the RGB interface is in use.

RTNI[4:0]	Clocks per line
5'h00	Setting disabled
⋮	⋮
5'h0F	Setting disabled
5'h10	16clocks
5'h11	17 clocks
5'h12	18 clocks
⋮	⋮
5'h1E	30 clocks
5'h1F	31 clocks

* 1 clock: Internal operation clock (fiosc)

DIVI[1:0]	Division ratio	Internal operation clock frequency (fiosc)
2'h0	1/1	fosc ÷ 1
2'h1	1/2	fosc ÷ 2
2'h2	1/4	fosc ÷ 4
2'h3	1/8	fosc ÷ 8

* fosc: CR oscillation frequency

Formula to calculate a frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Number or clock per line} \times \text{Division ratio} \times (\mathit{Line} + \mathit{FP} + \mathit{BP})} \text{ [Hz]}$$

fosc : CR oscillation frequency
Line : Number of driven lines (NL bit)
Division ratio : DIVI bit
Number of clocks per line : RTNI bit
BP : Number of lines for back porch
FP : Number of lines for front porch

(15) External Display Interface Control 2 (R00Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVE [1]	DIVE [0]	0	RTNE [6]	RTNE [5]	RTNE [4]	RTNE [3]	RTNE [2]	RTNE [1]	RTNE [0]

RTNE [6:0] This sets the number of internal clocks per 1H (line) period. Set the value that represents the number of DOTCLKs input in a 1H period, divided by the division ratio.

DIVE [1:0] This sets the internal division ratio of DOTCLK.
The internal operation is performed according to the clocks divided by the internal division ratio DIVE[1:0].

RTNE[6:0]	Clocks per line
7'h00	Setting disabled
⋮	⋮
7'h0F	Setting disabled
7'h10	16 clocks
7'h11	17 clocks
7'h12	18 clocks
⋮	⋮
7'h1E	126 clocks
7'h1F	127 clocks

1 clock: Internal operation clock (fdosc)

DIVE[1:0]	Division ratio	Internal operation clock frequency (fdosc)
2'h0	Setting disabled	
2'h1	1/4	fdotclk ÷ 4
2'h2	1/8	fdotclk ÷ 8
2'h3	1/16	fdotclk ÷ 16

fdotclk: DOTCLK frequency

(16) External Display Interface Control 3 (R00Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

DPL This sets the polarity of the signal on the DOTCLK pin.
- DPL = 0 : Inputs data on the rising edge of DOTCLK.
- DPL = 1 : Inputs data on the falling edge of DOTCLK.

EPL This sets the polarity of the signal on the ENABLE pin.
- EPL = 0 : Data is written to PD17-0 when ENABLE = Low.
  : No data is written when ENABLE = High.
- EPL = 1 : Data is written to PD17-0 when ENABLE = High.
  : No data is written when ENABLE = Low.

HSPL This sets the polarity of the signal on the HSYNC pin.
- HSPL = 0 : Low active.
- HSPL = 1 : High active.

VSPL This sets the polarity of the signal on the VSYNCE pin.
- VSPL = 0 : Low active.
- VSPL = 1 : High active.

(17) Source Driver Control 1 (R012h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTI [1]	SDTI [0]

SDTI [1:0] This sets the point of source output (S1-S720) when operation mode (DM = 2'h0 or 2'h2) is performed by the internal clock.

SDTI [1:0]	Source output point
2'h0	1 clock
2'h1	2 clocks
2'h2	3 clocks
2'h3	4 clocks

Clock: Internal operation clock (according to CR oscillation frequency and DIVI[1:0])

(18) Gate Driver Control 1 (R013h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	DPTI [2]	DPTI [1]	DPTI [0]

DPTI [2:0] This sets the non-overlap time of the gate output when operation mode (DM = 2'h0 or 2'h2) is performed by the internal clock.

SDTI [1:0]	Gate output non-overlap time
3'h0	0 clocks
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

* Clock: Internal operation clock (according to CR oscillation frequency and DIVI[1:0])

Note that the absolute times of the clocks set in the above SDTI[1:0] and DPTI[1:0] vary according to the oscillation frequency of the internal oscillation circuit.

(19) Source Driver Control 2 (R018h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTE [2]	SDTE [1]	SDTE [0]

SDTE [2:0] This sets the point of source output (S1-S720) when operation mode (DM = 2'h1) is performed by the RGB interface (DOTCLK).

SDTE [2:0]	Source output point
2'h0	1 clock
2'h1	2 clocks
2'h2	3 clocks
2'h3	4 clocks
2'h4	5 clocks
2'h5	6 clocks
2'h6	7 clocks
2'h7	Setting disabled

* Clock: Internal operation clock (according to DOTCLK frequency and DIVE[1:0])

(20) Gate Driver Control 2 (R019h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	DPTE [2]	DPTE [1]	DPTE [0]

DPTE [2:0] This sets the non-overlap time of the gate output when the operation mode (DM = 2'h1) is performed by the RGB interface (DOTCLK).

DPTE[2:0]	Gate driver control 2 (R019h)
3'h0	0 clocks
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

* Clock: Internal operation clock (according to DOTCLK frequency and DIVE[1:0])

Note that the absolute times of the clocks set in the above SDTE [1:0] and DPTE [2:0] vary according to the oscillation frequency of the internal oscillation circuit.

■ **Power control instructions**

(1) Power Control 1 (R100h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	GON	COM	PON	0	0	0	SAP	0	0	AP [1]	AP [0]	0	DSTB	SLP	0

SLP Sets sleep mode. When SLP = 1, all the bits of AP [1:0] and SAP are fixed to "0" to stop the power supply circuit operation. These bits are not rewritten. In sleep mode, the oscillator and VDD regulator are in operation.

DSTB Deep standby mode is entered when DSTB = 1. GRAM data and instruction settings are destroyed during deep standby mode and must be reset after releasing deep standby mode.

AP [1:0] This controls the on/off of DCCLK operation of the step-up clock and power supply circuit. Setting AP [1:0]≠2'h0 starts DCCLK operation. Setting AP[1:0] = 2'h0 stops DCCLK operation. AP [1:0] also adjusts the constant current for the operational amplifier circuit. A larger constant current stabilizes the operational amplifier circuit. Take the stability of each level and power consumption into account when adjusting.
AP [1:0] is one of the power on/off instructions. Always follow the power supply setting sequence when setting AP [1:0].

AP [1:0]	Current in operational amplifier
2'h0	Operational amplifiers and step-up circuits: stopped
2'h1	Constant current in operational amplifier: small
2'h2	Constant current in operational amplifier: medium
2'h3	Setting disabled

SAP This controls the on/off of the gradation voltage generator circuit. Setting SAP = 0 stops the circuit operation. Setting SAP = 1 starts the circuit operation.
SAP is one of the power on/off instructions. Always follow the power supply setting sequence when setting SAP.

PON This controls the start/stop of outputting VGH, VGL, and VCL. Setting PON = 0 stops outputting. Setting PON = 1 starts outputting.
PON is one of the power on/off instructions. Always follow the power supply setting sequence when setting PON.

COM This controls the start/stop of Vcom output.
COM is one of the power on/off instructions. Always follow the power supply setting sequence when setting COM.

GON This sets Vcom output and G1-G320 output.
When GON = 0, the Vcom output level becomes GND.
The state of G1-G320 output is defined according to the DTE and GON bits as shown below.

DTE	GON	Gate output
0	0	VGH
0	1	VGL
1	0	VGH
1	1	VGH/VGL (Normal operation)

(2) Power Control 2 (R101h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	DRVE [3]	DRVE [2]	DRVE [1]	DRVE [0]	0	0	0	ORDCCK

ORDCCK This is used to switch the reference clocks to generate a step-up clock DCCLK.
When ORDCCK is set to "0", a signal is generated in accordance with the internal oscillation clock.
When ORDCCK is set to "1", a signal is generated in accordance with DOTCLK. The step-up clock division ratio is controlled by DRVE[3:0].

DRVE [3:0] This represents the division ratio when DCCLK is generated in accordance with DOTCLK.
The display quality and power consumption must be taken into account to perform the optimum setting.

DRVE				Setting		Remarks
3	2	1	0	RIM=0	RIM=1	
0	0	0	0	110 Dotclk	330 Dotclk	Duty setting when DCCLK is synchronized with CL1 and in the same cycle.
0	0	0	1	120 Dotclk	360 Dotclk	
0	0	1	0	130 Dotclk	390 Dotclk	
0	0	1	1	140 Dotclk	420 Dotclk	
0	1	0	0	150 Dotclk	450 Dotclk	
0	1	0	1	160 Dotclk	480 Dotclk	
0	1	1	0	1/210	1/630	Setting when DCCLK is generated by DOTCLK division non-synchronous with CL1.
0	1	1	1	1/130	1/390	
1	0	0	0	1/100	1/300	
1	0	0	1	1/80	1/240	
1	0	1	0	1/70	1/210	
1	0	1	1	1/64	1/192	
1	1	0	0	1/52	1/156	
1	1	0	1	1/44	1/132	
1	1	1	0	1/36	1/108	
1	1	1	1	1/32	1/96	

(3) Power Control 3 (R102h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	CA	VCOMG	DC1 [3]	DC1 [2]	DC1 [1]	DC1 [0]	0	DC0 [2]	DC0 [1]	DC0 [0]	0	0	DC [4]	DC [3]

DC [4:3] This sets the frequency of step-up clock DCCLK. A higher step-up operating frequency enhances the driving capacity of step-up circuits and the quality of display, but power consumption increases. Take display quality and current consumption into account when adjusting.

DC [4:3]	Division ratio to oscillation frequency
2'h0	1/4
2'h1	1/8
2'h2	1/16
2'h3	1/32

DC0 [2:0] This sets the step-up cycle of step-up circuits 1 and 3 corresponding to the DCCLK set with the DC [4:3]. A higher step-up frequency enhances the driving capacity of step-up circuits, but power consumption increases. Take display quality and current consumption into account when adjusting.

DC0 [2:0]	Step-up cycle in step-up circuit 1	Step-up cycle in step-up circuit 3
3'h0	DCCLK	DCCLK divided by 2
3'h1	DCCLK	DCCLK divided by 4
3'h2	DCCLK	DCCLK divided by 8
3'h3	DCCLK divided by 2	DCCLK divided by 4
3'h4	DCCLK divided by 2	DCCLK divided by 8
3'h5	DCCLK divided by 4	DCCLK divided by 8
3'h6	DCCLK divided by 8	DCCLK divided by 16
3'h7	Setting disabled	Setting disabled

DC1 [3:0] This sets the step-up cycle of step-up circuit 2 corresponding to the DCCLK set with the DC [4:3]. A higher step-up frequency enhances the driving capacity of the step-up circuit, but power consumption increases. Take display quality and current consumption into account when adjusting. Since CL1 is used as the step-up clock when DC1 [3] = 1, always input CL1 (D [1:0]≠00) before the setting.

DC1 [3:0]	Step-up cycle in step-up circuit 2
4'h0	DCCLK
4'h1	DCCLK divided by 2
4'h2	DCCLK divided by 4
4'h3	DCCLK divided by 8
4'h4	DCCLK divided by 16
4'h5	DCCLK divided by 32
4'h6	Setting disabled
4'h7	Setting disabled
4'h8	CL1
4'h9	CL1 divided by 2
4'hA	CL1 divided by 4
4'hB	CL1 divided by 8
4'hC	CL1 divided by 16
4'hD	CL1 divided by 32
4'hE	Setting disabled
4'hF	Setting disabled

VCOMG When VCOMG = 1, the output level of VcomL can be set with the instruction “VDV”. Capacitors are required on VcomL, VCL, and between C31+ and C31-.
VCOMG = 1 is enabled when PON = 1. When VCOMG = 0, the VcomL output is fixed to GND and the instruction “VDV” becomes invalid.
When VCOMG = 0, the VcomL output and VCL output stop, so capacitors are not required on VcomL, VCL, or between C31+ and C31-.

CA This controls the operation mode of the step-up circuit 1 (DDVDH).
CA = 0: Low load drive mode
CA = 1: Normal mode. A capacitor is required between the C1A+ and C1A- pins.
When CA = 0, the current consumption of the step-up circuit 1 (DDVDH) decreases, but the driving capacity also decreases. Take the DDVDH output level into account when setting CA.

(4) Power Control 4 (R103h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VRD [3]	VRD [2]	VRD [1]	VRD [0]	0	0	APR [1]	APR [0]	0	0	BT [1]	BT [0]	0	0	VC [1]	VC [0]

VC [1:0] This sets the VciOUT output on the basis of reference voltage.
When AP [1:0]≠2'h0 and VC [1:0]≠3'h0, a capacitor is required on the VciOUT pin to stabilize the VciOUT operational amplifier circuit. When VC [1:0] = 3'h0, the VciOUT operational amplifier circuit stops, so a capacitor is not required on the VciOUT pin.

VC [1:0]	VciOUT voltage
2'h0	1.00×REFVcc
2'h1	0.925×REFVcc
2'h2	0.875×REFVcc
2'h3	Setting disabled

Note: Set the VciOUT voltage so that the voltage DDVDH-GND is 6.0V or below.

BT [1:0] This controls the step-up magnification of VGH. Adjust the step-up magnification according to the power supply voltage in use.

BT [1:0]	VGH output	Capacitor connection pin
2'h0	VDCDC2×2+VciOUT	VGH, C21±, C22±
2'h1	VDCDC×2	VGH, C21±
2'h2	VDCDC×3	VGH, C21±, C22±
2'h3	Setting disabled	Setting disabled

APR [1:0] This adjusts the constant current of the constant current source and controls the operation/stop of the operational amplifier of the VDCDC2 output circuit.
When AP[1:0]≠2'h0 and APR[1:0]≠2'h0, a capacitor is required on the VDCDC2 pin to stabilize the VDCDC2 operational amplifier circuit. A larger constant current stabilizes the operational amplifier circuit. Take the stability of the VDCDC2 output and power consumption into account when adjusting. The VDCDC2 output voltage is set with the instruction VRD [3:0].
When the VDCDC2 output level is used as the DDVDH, set APR [1:0] = 2'h0. At this time, the instruction VRD [3:0] is invalid. When APR [1:0] = 2'h0, the operational amplifier of the output circuit stops, so a capacitor is not required on VDCDC2 pin.

APR [1:0]	Current in VDCDC2 operational amplifier
2'h0	VDCDC2 output circuit: stopped (DDVDH output)
2'h1	Constant current in operational amplifier: small
2'h2	Constant current in operational amplifier: medium
2'h3	Setting disabled

VRD [3:0] This sets the VDCDC2 output on the basis of reference voltage.

VRD [3:0]	VDCDC2 voltage
4'h0	Setting disabled
4'h1	Setting disabled
4'h2	Setting disabled
4'h3	Setting disabled
4'h4	Setting disabled
4'h5	Setting disabled
4'h6	Setting disabled
4'h7	Setting disabled
4'h8	1.60×REFVcc
4'h9	Setting disabled
4'hA	1.70×REFVcc
4'hB	Setting disabled
4'hC	1.80×REFVcc
4'hD	Setting disabled
4'hE	Setting disabled
4'hF	Setting disabled

Note: Set the VDCDC2 voltage so that the voltage VGH-GND is 13.0V or below and the voltage VGL-GND is -5.0V or above.

(5) Power Control 5 (R110h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VDV [3]	VDV [2]	VDV [1]	VDV [0]	VRH [3]	VRH [2]	VRH [1]	VRH [0]

VRH [3:0] This sets the amplitude of the alternating voltage VDH on the basis of REFVcc.

VRH[3:0]	VDH Voltage
4'h0	1.20×REFVcc
4'h1	1.25×REFVcc
4'h2	1.30×REFVcc
4'h3	1.35×REFVcc
4'h4	1.40×REFVcc
4'h5	1.45×REFVcc
4'h6	1.50×REFVcc
4'h7	1.55×REFVcc
4'h8	1.60×REFVcc
4'h9	1.65×REFVcc
4'hA	1.70×REFVcc
4'hB	1.75×REFVcc
4'hC	1.80×REFVcc
4'hD	1.85×REFVcc
4'hE	1.90×REFVcc
4'hF	Setting disabled

VDV [3:0] This sets the amplitude of the alternating voltage Vcom on the basis of VDH.

VDV[3:0]	Vcom amplitude
4'h0	Setting disabled
4'h1	Setting disabled
4'h2	Setting disabled
4'h3	1.11×VDH
4'h4	1.08×VDH
4'h5	1.05×VDH
4'h6	1.02×VDH
4'h7	0.99×VDH
4'h8	0.96×VDH
4'h9	0.93×VDH
4'hA	Setting disabled
4'hB	Setting disabled
4'hC	Setting disabled
4'hD	Setting disabled
4'hE	Setting disabled
4'hF	Setting disabled

Note: The Vcom amplitude must be 6V or below

(6) Power Control 6 (R111h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	CLU [1]	CLU [0]	CHU [1]	CHU [0]

CHU [1:0] This sets the low impedance mode of VcomH. A larger current in the operational amplifier stabilizes the circuit operation. Take the stability of VcomH and the power consumption into account when adjusting.

CLU [1:0] This sets the low impedance mode of VcomL. A larger current in the operational amplifier stabilizes the circuit operation. Take the stability of VcomL and the power consumption into account when adjusting

CHU[1:0]	VcomH output	Current in operational amplifier
2'h0	Normal	According to AP bit
2'h1	Low impedance	Constant current: small
2'h2	Low impedance	Constant current: medium
2'h3	Setting disabled	Setting disabled

CLU[1:0]	VcomL output	Current in operational amplifier
2'h0	Normal	According to AP bit
2'h1	Low impedance	Constant current: small
2'h2	Low impedance	Constant current: medium
2'h3	Setting disabled	Setting disabled

■ **GRAM access instructions**

(1) RAM Address Set (Horizontal Address) (R200h)

(2) RAM Address Set (Vertical Address) (R201h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	AD [7]	AD [6]	AD [5]	AD [4]	AD [3]	AD [2]	AD [1]	AD [0]
W	1	0	0	0	0	0	0	0	AD [16]	AD [15]	AD [14]	AD [13]	AD [12]	AD [11]	AD [10]	AD [9]	AD [8]

AD [16:0] his initializes the GRAM address in the Address Counter (AC). The address counter (AC) is automatically updated in accordance with the AM and I/D bits after data is written to the GRAM. This makes it possible to write data consecutively without resetting addresses. The address is not automatically updated when data is read from the GRAM.

Note 1: When the RGB interface is selected (RM = 1), the address AD[16:0] is set in the address counter every frame on the following edge.

VSPL = 0: on the falling edge of VSYNC

VSPL = 1: on the rising edge of VSYNC

Note 2: When the internal clock operation and VSYNC interface is selected (RM = 0), the address is set when an instruction is executed.

[GRAM address range]

AD[16:0]	GRAM data setting
17'h00000 ~ 17'h000EF	Bitmap data for G1
17'h00100 ~ 17'h001EF	Bitmap data for G2
17'h00200 ~ 17'h002EF	Bitmap data for G3
17'h00300 ~ 17'h003EF	Bitmap data for G4
⋮	⋮
17'h13C00 ~ 17'h13CEF	Bitmap data for G317
17'h13D00 ~ 17'h13DEF	Bitmap data for G318
17'h13E00 ~ 17'h13EEF	Bitmap data for G319
17'h13F00 ~ 17'h13FEF	Bitmap data for G320

(3) Write DATA to RAM (R202h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	The DB17-0 pins are assigned to RAM write data (WD[17:0]) according to the interface.															

WD [17:0] All GRAM write data is expanded into 18 bits internally before being written to the GRAM. Data is expanded into 18 bits differently according to the interface.

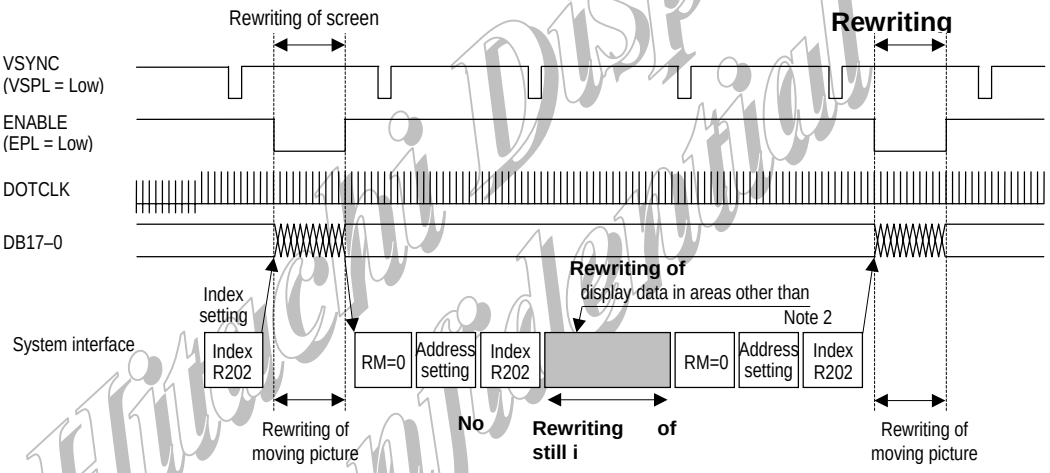
Gradation levels are selected according to the GRAM data. The GRAM addresses are automatically updated according to the AM and I/D bits after data is written to the GRAM. No access to the GRAM during standby mode is allowed. When an 8- or 16-bit interface mode is selected, the least significant bit of R data/B data is written with the same data as the most significant bit of R data/B data, and 65,536 colors are available.

- GRAM access from RGB interface or system interface

With the BD663474, all display data is stored in the internal GRAM even when an RGB interface is used. The RGB interface is therefore allowed to transfer only the data related to the moving picture area and the screen-rewriting frames. The above arrangement, combined with the high-speed write mode (HWM = 1) and the window address function, enables low power consumption and high-speed access during moving picture display. Except for the window-rewriting frames, the system interface allows rewriting display data in areas other than the moving picture area.

While the RGB interface is selected, writing of GRAM data is constantly taking place responding to DOTCLK as long as the ENABLE signal accepts writing. When writing data to the GRAM from the system interface, interrupt data writing from the RGB interface with the ENABLE signal.
When accessing the GRAM from the system interface, start from the RGB interface during the write/read bus time. If there is a conflict between the two interfaces in GRAM access, the validity of the written data is not guaranteed.

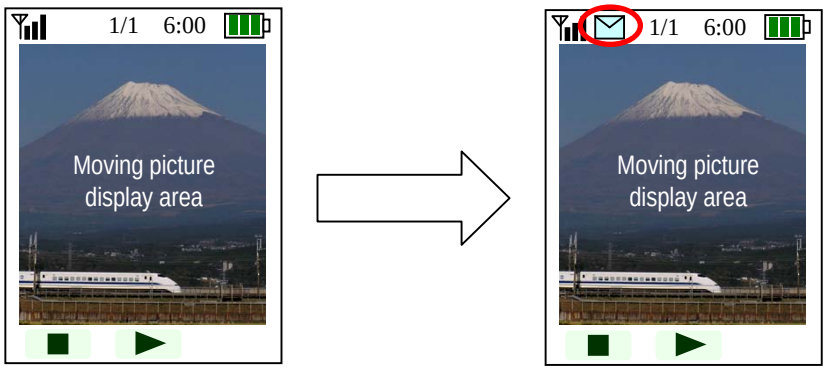
Example: Rewriting of still image area while moving pictures are displayed



Note 1: When an RGB interface is used, address setting is performed as follows:
When VSPL = 0: on every falling edge of VSYNC
When VSPL = 1: on every rising edge of VSYNC

Note 2: Address setting and index setting (R202h) must be performed before GRAM access from the RGB interface is started.

Note 3: The RGB interface must be used in high-speed write mode (HWM = 1).



(4) Read DATA from RAM (R202h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	DB17-0 pins are assigned to RAM read data (RD[17:0]) according to the interface.															

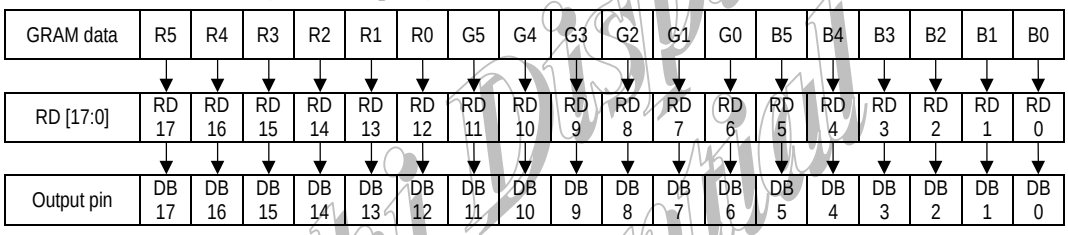
RD [17:0] This reads 18-bit data from the GRAM. The bit assignment between the data read out from the GRAM and DB[17:0] pins differs according to the interface. When data is read out from the GRAM to the microcomputer, the first word read immediately after the GRAM address setting is taken in the internal read data register and invalid data is sent to the data bus (DB17-0). Valid data is sent to the data bus as the second word data is read. Note that bit processing, such as logical operations, is implemented on an 18-bit basis.

When an 8- or 16-bit interface is selected, the least significant written bits of R data/B data can not be read out.

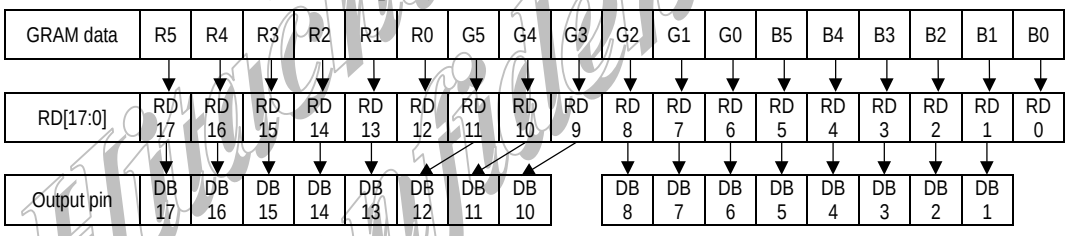
Note 1: This register is not available with the RGB interface.

Note 2: Set TRI = 0 when reading data.

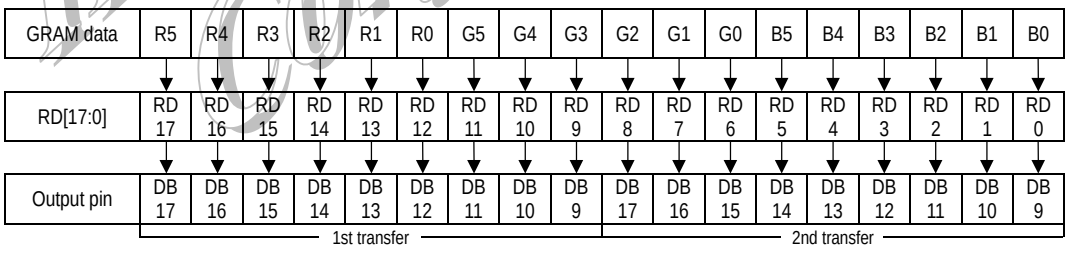
■ **80-series 18-bit interface (1 transfer/pixel)**



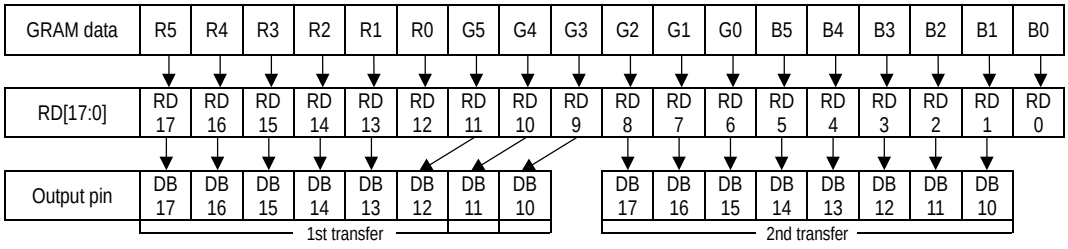
■ **80-series 16-bit interface (1 transfer/pixel)**



■ **80-series 9-bit interface (2 transfers/pixel)**



■ **80-series 8-bit interface / SPI (2 transfers/pixel)**



■ **80-series 8-bit interface (little-endian) (2 transfers/pixel)**

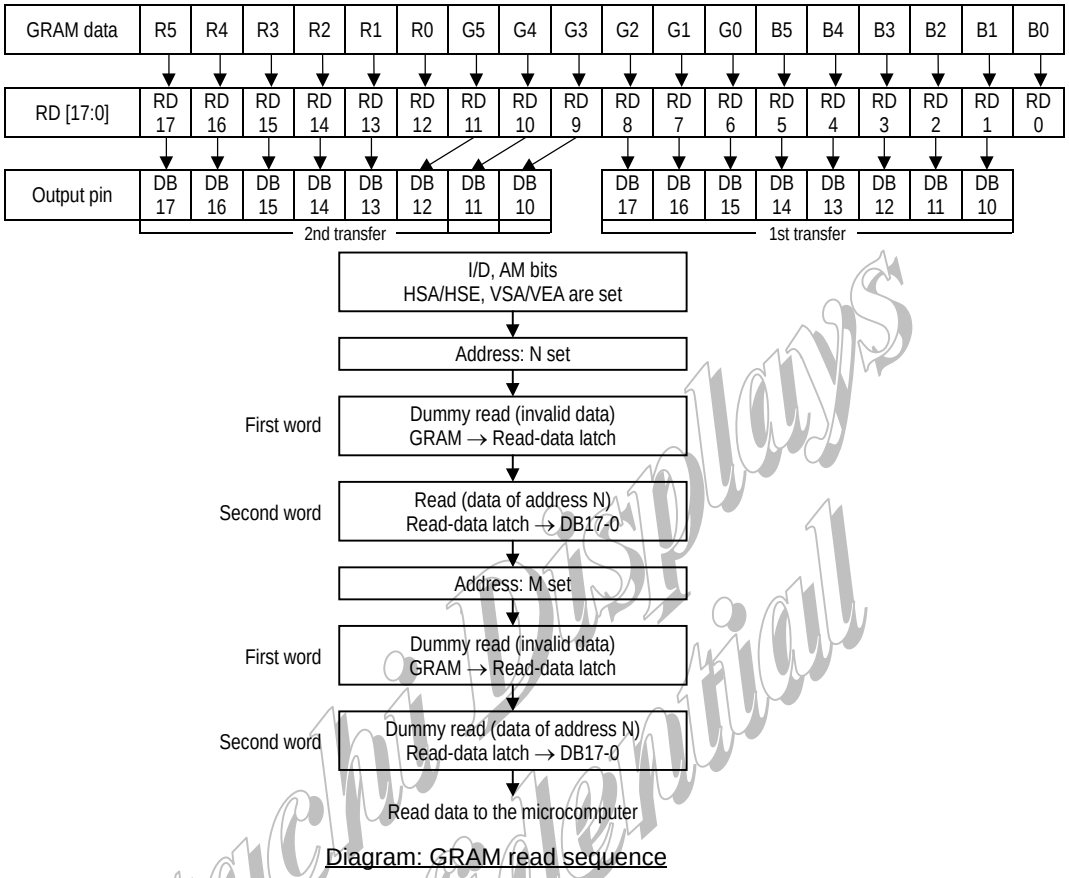


Diagram: GRAM read sequence

(5) RAM Write Data Mask 1 (R203h)

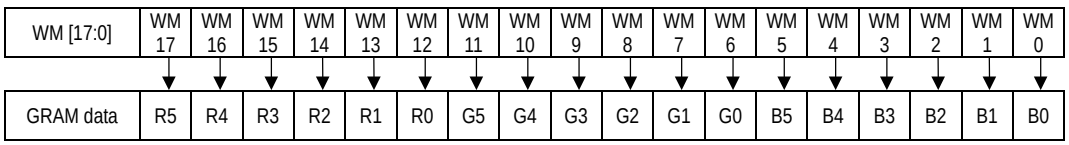
(6) RAM Write Data Mask 2 (R204h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	WM [11]	WM [10]	WM [9]	WM [8]	WM [7]	WM [6]	0	0	WM [5]	WM [4]	WM [3]	WM [2]	WM [1]	WM [0]
W	1	0	0	0	0	0	0	0	0	0	0	WM [17]	WM [16]	WM [15]	WM [14]	WM [13]	WM [12]

WM [17:0] This masks data in the bit unit when writing data to the GRAM. When WM17 = 1, for example, the most significant bit of the write data is masked so that writing to the GRAM data is not performed. In the same manner, when WM16 - WM0 bits are set to "1", the corresponding bits of the write data are masked.

The write mask function is performed on 18-bit GRAM write data.

Note: This function is not available with the RGB interface.



■ **Window address control instructions**

(1) Horizontal RAM Window Address Start Point (R210h)

(2) Horizontal RAM Window Address End Point (R211h)

(3) Vertical RAM Window Address Start Point (R212h)

(4) Vertical RAM Window Address End Point (R213h)

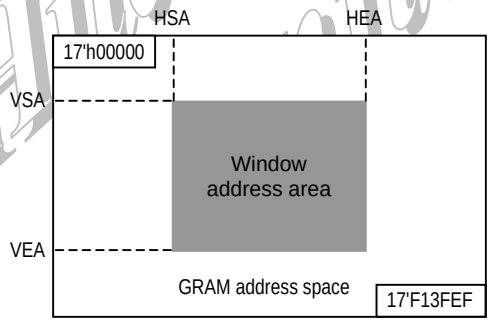
R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	HSA [7]	HSA [6]	HSA [5]	HSA [4]	HSA [3]	HSA [2]	HSA [1]	HSA [0]
W	1	0	0	0	0	0	0	0	0	HEA [7]	HEA [6]	HEA [5]	HEA [4]	HEA [3]	HEA [2]	HEA [1]	HEA [0]
W	1	0	0	0	0	0	0	0	VSA [8]	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]
W	1	0	0	0	0	0	0	0	VEA [8]	VEA [7]	VEA [6]	VEA [5]	VEA [4]	VEA [3]	VEA [2]	VEA [1]	VEA [0]

HSA [7:0] These represent the addresses of the start and end positions, respectively, of the window address area in the horizontal direction.

HEA [7:0] Data is written to the GRAM within the area set with HEA[7:0] from the address set with HSA [7:0]. The addresses must be set before the GRAM write operation.
When setting, make sure 8’h0 ≤ HSA[7:0] < HEA[7:0] ≤ 8’hEF, and HEA – HAS ≥ 8’h4.

VSA [8:0] These represent the addresses of the start and end positions, respectively, of the window address area in the vertical direction.

VEA [8:0] Data is written to the GRAM within the area set with VEA[8:0] from the address set with VSA [8:0]. The addresses must be set before the GRAM write operation.
When setting, make sure 9’h0 ≤ VSA[8:0] < VEA[8:0] ≤ 9’h13F.



Window address setting range

8'h0 ≤ HAS[7:0] < HEA[7:0] ≤ 8'hEF

HEA–HAS ≥ 8'h4

9'h0 ≤ HAS VSA[8:0] < VEA[8:0] ≤ 9'h13F

Note 1: Make a window address area within the GRAM address area.

Note 2: In high-speed write mode, data is written in units of horizontal lines. Always perform GRAM data write in units of lines.

Note 3: Always set the address within the window address area. In high-speed write mode, set the address at the start of a line within the window address area.

■ **Window address control instructions for moving picture**

(1) Horizontal RAM Window Address Start Point for Moving Picture Control (R214h)

(2) Horizontal RAM Window Address End Point for Moving Picture Control (R215h)

(3) Vertical RAM Window Address Start Point for Moving Picture Control (R216h)

(4) Vertical RAM Window Address End Point for Moving Picture Control (R217h)

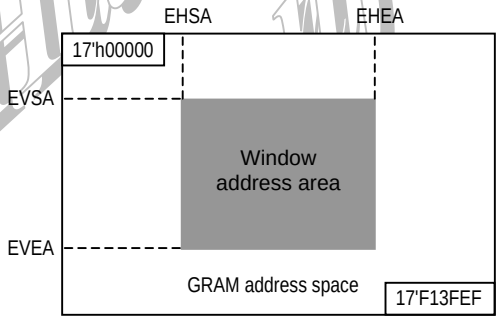
R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	EHSA [7]	EHSA [6]	EHSA [5]	EHSA [4]	EHSA [3]	EHSA [2]	EHSA [1]	EHSA [0]
W	1	0	0	0	0	0	0	0	0	EHEA [7]	EHEA [6]	EHEA [5]	EHEA [4]	EHEA [3]	EHEA [2]	EHEA [1]	EHEA [0]
W	1	0	0	0	0	0	0	0	EVSA [8]	EVSA [7]	EVSA [6]	EVSA [5]	EVSA [4]	EVSA [3]	EVSA [2]	EVSA [1]	EVSA [0]
W	1	0	0	0	0	0	0	0	EVEA [8]	EVEA [7]	EVEA [6]	EVEA [5]	EVEA [4]	EVEA [3]	EVEA [2]	EVEA [1]	EVEA [0]

EHSA [7:0] These represent the addresses of the start and end positions, respectively, of the window address area for moving picture control in the horizontal direction.

EHEA [7:0] Moving picture control is performed on the data within the area set with EHEA [7:0] from the address set with EHSA [7:0]. The addresses must be set before the GRAM write operation.
When setting, make sure 8'h0 ≤ HSA ≤ EHSA[7:0] < EHEA[7:0] ≤ HEA ≤ 8'hEF, and EHEA – EHSA ≥ 8'h4.

EVSA [8:0] These represent the addresses of the start and end positions, respectively, of the window address area for moving picture control in the vertical direction.

EVEA [8:0] Data within the area set with EVEA [8:0] from the address set with EVSA [8:0]. The addresses must be set before the GRAM write operation.
In setting, make sure 9'h0 ≤ VSA ≤ EVSA[8:0] < EVEA[8:0] ≤ VEA ≤ 9'h13F



Window address setting range

8'h0 ≤ HSA ≤ EHSA < EHEA ≤ HEA ≤ 8'hEF
EHEA–EHSA≥ 8'h4

9'h0 ≤ VSA ≤ EVSA < EVEA ≤ VEA ≤ 9'h13F

■ **γ control instructions**

(1) Gamma Control (R300h ~ R309h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	PKP 3[2]	PKP 3[1]	PKP 3[0]	0	PKP 2[2]	PKP 2[1]	PKP 2[0]	0	PKP 1[2]	PKP 1[1]	PKP 1[0]	0	PKP 0[2]	PKP 0[1]	PKP 0[0]
W	1	0	PRP 3[2]	PRP 3[1]	PRP 3[0]	0	PRP 2[2]	PRP 2[1]	PRP 2[0]	0	PRP 1[2]	PRP 1[1]	PRP 1[0]	0	PRP 0[2]	PRP 0[1]	PRP 0[0]
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	PRP 4[2]	PRP 4[1]	PRP 4[0]
W	1	0	PRP 8[2]	PRP 8[1]	PRP 8[0]	0	PRP 7[2]	PRP 7[1]	PRP 7[0]	0	PRP 6[2]	PRP 6[1]	PRP 6[0]	0	PRP 5[2]	PRP 5[1]	PRP 5[0]
W	1	0	0	0	VRP 1[4]	VRP 1[3]	VRP 1[2]	VRP 1[1]	VRP 1[0]	0	0	0	0	VRP 0[3]	VRP 0[2]	VRP 0[1]	VRP 0[0]
W	1	0	PKN 3[2]	PKN 3[1]	PKN 3[0]	0	PKN 2[2]	PKN 2[1]	PKN 2[0]	0	PKN 1[2]	PKN 1[1]	PKN 1[0]	0	PKN 0[2]	PKN 0[1]	PKN 0[0]
W	1	0	PRN 3[2]	PRN 3[1]	PRN 3[0]	0	PRN 2[2]	PRN 2[1]	PRN 2[0]	0	PRN 1[2]	PRN 1[1]	PRN 1[0]	0	PRN 0[2]	PRN 0[1]	PRN 0[0]
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	PRN 4[2]	PRN 4[1]	PRN 4[0]
W	1	0	PRN 8[2]	PRN 8[1]	PRN 8[0]	0	PRN 7[2]	PRN 7[1]	PRN 7[0]	0	PRN 6[2]	PRN 6[1]	PRN 6[0]	0	PRN 5[2]	PRN 5[1]	PRN 5[0]
W	1	0	0	0	VRN 1[4]	VRN 1[3]	VRN 1[2]	VRN 1[1]	VRN 1[0]	0	0	0	0	VRN 0[3]	VRN 0[2]	VRN 0[1]	VRN 0[0]

PKP3–0 [2:0] γ fine adjustment register for positive polarity

PRP8–0 [2:0] Gradient adjustment register for positive polarity

VRP1 [4:0], VRP0 [3:0] Amplitude adjustment register for positive polarity

PKN3–0 [2:0] γ fine adjustment register for negative polarity

PRN8–0 [2:0] Gradient adjustment register for negative polarity

VRN1 [4:0], VRN0 [3:0] Amplitude adjustment register for negative polarity

■ **Display-system instructions**

(1) Gate Driver Output Control (R400h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	GS	SM	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]	0	0	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]

NL [5:0] This sets the number of lines to drive liquid crystal. The number of lines can be set in multiples of 8 (with a minimum number of 16). Set more than the number of lines for the full size of the panel in use.

NL [5:0]	Number of driven lines
6'h00	Setting disabled
6'h01	16 lines
6'h02	24 lines
6'h03	32 lines
6'h04	40 lines
6'h05	48 lines
6'h06	56 lines
6'h07	64 lines
6'h08	72 lines
6'h09	80 lines
6'h0A	88 lines
6'h0B	96 lines
6'h0C	104 lines
6'h0D	112 lines
6'h0E	120 lines
6'h0F	128 lines
6'h10	136 lines
6'h11	144 lines
6'h12	152 lines
6'h13	160 lines

NL [5:0]	Number of driven lines
6'h14	168 lines
6'h15	176 lines
6'h16	184 lines
6'h17	192 lines
6'h18	200 lines
6'h19	208 lines
6'h1A	216 lines
6'h1B	224 lines
6'h1C	232 lines
6'h1D	240 lines
6'h1E	248 lines
6'h1F	256 lines
6'h20	264 lines
6'h21	272 lines
6'h22	280 lines
6'h23	288 lines
6'h24	296 lines
6'h25	304 lines
6'h26	312 lines
6'h27	320 lines
6'h28-6'h3F	Setting disabled

SCN[5:0] This sets the position for the gate driver to start scanning gate lines.

GS This sets the scan direction of the gate line.

SM This sets the scan sequence of the gate line in combination with the GS bit. Refer to the gate scan mode function for details.

SCN[5:0]	Start position for the gate-line output			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
6'h00	G1	G320	G1	G320
6'h01	G9	G312	G17	G304
6'h02	G17	G304	G33	G288
6'h03	G25	G296	G49	G272
6'h04	G33	G288	G65	G256
6'h05	G41	G280	G81	G240
6'h06	G49	G272	G97	G224
6'h07	G57	G264	G113	G208
6'h08	G65	G256	G129	G192
6'h09	G73	G248	G145	G176
6'h0A	G81	G240	G161	G160
6'h0B	G89	G232	G177	G144
6'h0C	G97	G224	G193	G128
6'h0D	G105	G216	G209	G112
6'h0E	G113	G208	G225	G96
6'h0F	G121	G200	G241	G80
6'h10	G129	G192	G257	G64
6'h11	G137	G184	G273	G48
6'h12	G145	G176	G289	G32
6'h13	G153	G168	G305	G16
6'h14	G161	G160	G2	G319
6'h15	G169	G152	G18	G303
6'h16	G177	G144	G34	G287
6'h17	G185	G136	G50	G271
6'h18	G193	G128	G66	G255
6'h19	G201	G120	G82	G239
6'h1A	G209	G112	G98	G223
6'h1B	G217	G104	G114	G207
6'h1C	G225	G96	G130	G191
6'h1D	G233	G88	G146	G175
6'h1E	G241	G80	G162	G159
6'h1F	G249	G72	G178	G143
6'h20	G257	G64	G194	G127
6'h21	G265	G56	G210	G111
6'h22	G273	G48	G226	G95
6'h23	G281	G40	G242	G79
6'h24	G289	G32	G258	G63
6'h25	G297	G24	G274	G47
6'h26	G305	G16	G290	G31
6'h27-6'h3F	Setting disabled			

(2) Display Control (R401h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VLE	REV

REV When REV = 1, the image in the display area is inversed. An inversed gradation level allows both normally black and normally white panels to be displayed with the same data.
The source outputs during the front/back porches and the non-display area in the partial display mode are set with the PTS setting.

REV	RAM data	Source output level in display area	
		Positive polarity	Negative polarity
0	18'h00000	V63	V0
	⋮	⋮	⋮
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	⋮	⋮	⋮
	18'h3FFFF	V63	V0

VLE A vertical scroll display is enabled when VLE = 1. The VL setting determines the first line to be displayed. VL[8:0] sets the amount of scrolling, i.e. the number of lines to be shifted from the first line. Vertical scrolling is not available in external display interface mode. In this case, set VLE0 to "0".

VLE	Display on screen
0	Fixed display
1	Scrolling display

(3) RAM Address (Start Line) for Base Image (R402h)

(4) RAM Address (End Line) for Base Image (R403h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	BSA [8]	BSA [7]	BSA [6]	BSA [5]	BSA [4]	BSA [3]	BSA [2]	BSA [1]	BSA [0]
W	1	0	0	0	0	0	0	0	BEA [8]	BEA [7]	BEA [6]	BEA [5]	BEA [4]	BEA [3]	BEA [2]	BEA [1]	BEA [0]

BSA [8:0] These set the start line address (BSA) and the end line address (BEA) of the base image GRAM area.

BEA [8:0] Values set to BSA and BEA must be equal to or more than the lines required for driving the panel (NL). Make sure BEA – BSA ≥ NL. When BEA – BSA < NL, any area outside the designated area becomes a non-display area.

(5) Vertical Scroll Control for Base Image (R404h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	VL [8]	VL [7]	VL [6]	VL [5]	VL [4]	VL [3]	VL [2]	VL [1]	VL [0]

VL [8:0] This sets the amount of scrolling in the base image. The number of lines set with VL represents the amount of scrolling.

VL[8:0]	Amount of scrolling
9'h000	0 lines
9'h001	1 line
9'h002	2 lines
⋮	⋮
9'h13D	317 lines
9'h13E	318 lines
9'h13F	319 lines

Note: Do not set to more than 319 lines (VL = 9'h13F).

■ **Partial display control instruction**

(1) Display Position for Partial image1 (R500h)
(2) RAM Address (Start Line) for Partial Image1 (R501h)
(3) RAM Address (End Line) for Partial Image1 (R502h)
(4) Display Position for Partial image2 (R503h)
(5) RAM Address (Start Line) for Partial Image2 (R504h)
(6) RAM Address (End Line) for Partial Image2 (R505h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	PTDP0 [8]	PTDP0 [7]	PTDP0 [6]	PTDP0 [5]	PTDP0 [4]	PTDP0 [3]	PTDP0 [2]	PTDP0 [1]	PTDP0 [0]
W	1	0	0	0	0	0	0	0	PTSA0 [8]	PTSA0 [7]	PTSA0 [6]	PTSA0 [5]	PTSA0 [4]	PTSA0 [3]	PTSA0 [2]	PTSA0 [1]	PTSA0 [0]
W	1	0	0	0	0	0	0	0	PTEA0 [8]	PTEA0 [7]	PTEA0 [6]	PTEA0 [5]	PTEA0 [4]	PTEA0 [3]	PTEA0 [2]	PTEA0 [1]	PTEA0 [0]
W	1	0	0	0	0	0	0	0	PTDP1 [8]	PTDP1 [7]	PTDP1 [6]	PTDP1 [5]	PTDP1 [4]	PTDP1 [3]	PTDP1 [2]	PTDP1 [1]	PTDP1 [0]
W	1	0	0	0	0	0	0	0	PTSA1 [8]	PTSA1 [7]	PTSA1 [6]	PTSA1 [5]	PTSA1 [4]	PTSA1 [3]	PTSA1 [2]	PTSA1 [1]	PTSA1 [0]
W	1	0	0	0	0	0	0	0	PTEA1 [8]	PTEA1 [7]	PTEA1 [6]	PTEA1 [5]	PTEA1 [4]	PTEA1 [3]	PTEA1 [2]	PTEA1 [1]	PTEA1 [0]

PTDP0 [8:0] This represents the display position for the partial image 1.

PTDP1 [8:0] This represents the display position for the partial image 2.

PTSA0 [8:0] This sets the address of the RAM area start position for the partial image 1.

PTEA0 [8:0] This sets the address of the RAM area end position for the partial image 1.

PTSA1 [8:0] This sets the address of the RAM area start position for the partial image 2.

PTEA1 [8:0] This sets the address of the RAM area end position for the partial image 2.

Set the display areas of partial images 1 and 2 so that they do not overlap.

The partial image 1 display area = PTDP0, PTDP0+ (PTEA0 – PTSA0)

The partial image 2 display area = PTDP1, PTDP1+ (PTEA1 – PTSA1)

The following relation must be observed: Partial image 1 display area < Partial image 2 display area.

■ Instruction list

Main category		Sub category		Upper code								Lower code								Notes
Upper Index		Index		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
—	Index	—	Index	—	—	—	—	—	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
SR	Status read	—	Status read	0	0	0	0	0	0	0	0	0	L6	L5	L4	L3	L2	L1	L0	
0**	Display control system	000h	Start oscillation	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	*	
			Device code read	0	0	1	1	0	1	0	0	0	1	1	1	0	1	0	0	3474h
		001h	Driver output control	— 0	— 0	— 0	— 0	— 0	— 0	— 0	SS 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	0000h
		002h	Liquid crystal drive inversion control	— 0	— 0	— 0	— 0	— 0	— 0	B/C 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	NW[1] 0	NW[0] 0	0000h
		003h	Entry mode	TRI 0	DFM 0	— 0	BGR 0	— 0	— 0	HWM 0	— 0	— 0	— 0	ID[1] 1	ID[0] 1	AM 0	— 0	— 0	— 0	0030h
		004h	Resizing control	— 0	— 0	— 0	— 0	— 0	— 0	RCV[1] 0	RCV[0] 0	— 0	— 0	RCH[1] 0	RCH[0] 0	— 0	— 0	RSR[1] 0	RSR[0] 0	0000h
		005h	Setting disabled	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		006h	Moving image display control	— 0	— 0	— 0	— 0	— 0	— 0	COE[4] 0	COE[3] 0	— 0	COE[2] 0	COE[1] 0	COE[0] 0	— 0	— 0	EEE[1] 0	EEE[0] 0	0000h
		007h	Display control (1)	— 0	— 0	PTDE[1] 0	PTDE[0] 0	— 0	— 0	— 0	BASEE 0	— 0	— 0	— 0	DTE 0	— 0	— 0	D[1] 0	D[0] 0	0000h
		008h	Display control (2)	— 0	— 0	— 0	— 0	FP[3] 1	FP[2] 0	FP[1] 0	FP[0] 0	— 0	— 0	— 0	— 0	BP[3] 1	BP[2] 0	BP[1] 0	BP[0] 0	0808h
		009h	Display control (3)	— 0	— 0	— 0	— 0	— 0	PTS[2] 0	PTS[1] 0	PTS[0] 0	— 0	— 0	PTG[1] 0	PTG[0] 0	— 0	— 0	ISC[1] 0	ISC[0] 0	0000h
		00Ah	Setting disabled	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		00Bh	Display control (4)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	CL 0	— 0	0000h
		00Ch	External display interface control (1)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	RM 0	— 0	— 0	DM[1] 0	DM[0] 0	— 0	— 0	RIM[1] 0	RIM[0] 0	0000h
		00Dh	Frame cycle adjustment control	— 0	— 0	— 0	— 0	— 0	— 0	DIVI[1] 0	DIVI[0] 0	— 0	— 0	— 0	RTNI[4] 1	RTNI[3] 0	RTNI[2] 0	RTNI[1] 0	RTNI[0] 0	0010h
		00Eh	External display interface control (2)	— 0	— 0	— 0	— 0	— 0	— 0	DIVE[1] 1	DIVE[0] 0	— 0	RTNE[6] 0	RTNE[5] 0	RTNE[4] 1	RTNE[3] 1	RTNE[2] 1	RTNE[1] 1	RTNE[0] 0	021Eh
		00Fh	External display interface control (3)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	VSPL 0	HSPL 0	— 0	EPL 0	DPL 0	0000h
		010h~ 011h	Setting disabled	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		012h	Source driver interface control (1)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	SDTI[1] 0	SDTI[0] 0	0000h
		013h	Gate driver interface control (2)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	DPTI[2] 0	DPTI[1] 0	DPTI[0] 0	0000h
		014h~ 017h	Setting disabled	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		018h	Source driver interface control (2)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	SDTE[2] 0	SDTE[1] 0	SDTE[0] 0	0000h
		019h	Gate driver interface control (2)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	DPTE[2] 0	DPTE[1] 0	DPTE[0] 0	0000h
		01Ah~ 0FFh	Setting disabled	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
1**	Power control system	100h	Power control (1)	— 0	GON 0	COM 0	PON 0	— 0	— 0	— 0	SAP 0	— 0	— 0	AP[1] 0	AP[0] 0	— 0	DSTB 0	SLP 0	— 0	0000h
		101h	Power control (2)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	DRVE[3] 1	DRVE[2] 0	DRVE[1] 0	DRVE[0] 0	— 0	— 0	— 0	ORDCCK 0	0080h
		102h	Power control (3)	— 0	— 0	CA 0	VCOMG 0	DC1[3] 0	DC1[2] 0	DC1[1] 0	DC1[0] 0	— 0	DC0[2] 0	DC0[1] 0	DC0[0] 0	— 0	— 0	DC[1] 0	DC[0] 0	0000h
		103h	Power control (4)	VRD[3] 0	VRD[2] 0	VRD[1] 0	VRD[0] 0	— 0	— 0	APR[1] 0	APR[0] 0	— 0	— 0	BT[1] 0	BT[0] 0	— 0	— 0	VC[1] 0	VC[0] 0	0000h
		104h~ 10Fh	Setting disabled	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		110h	Power control (5)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	VDV[3] 1	VDV[2] 0	VDV[1] 0	VDV[0] 0	VRH[3] 1	VRH[2] 0	VRH[1] 0	VRG[0] 0	0088h
		111h	Power control (6)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	CLU[1] 0	CLU[0] 0	CHU[1]] 0	CHU[0] 0	0000h
		112h~ 1FFh	Setting disabled	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	

Note) Do not access an index where setting is not assigned.

Main category		Sub category		Upper code								Lower code								Notes
Upper Index		Index		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
2**	RAM access system	200h	Horizontal RAM address set	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	AD[7] 0	AD[6] 0	AD[5] 0	AD[4] 0	AD[3] 0	AD[2] 0	AD[1] 0	AD[0] 0	0000h
		201h	Vertical RAM address set	— 0	— 0	— 0	— 0	— 0	— 0	— 0	AD[16] 0	AD[15] 0	AD[14] 0	AD[13] 0	AD[12] 0	AD[11] 0	AD[10] 0	AD[9] 0	AD[8] 0	0000h
		202h	RAM data write / read	RAM write data (WD17–0) or RAM read data (RD17–0)								* Bit assignment varies according to selected interface.								
		203h	RAM write data mask (1)	— 0	— 0	WM[11] 0	WM[10] 0	WM[9] 0	WM[8] 0	WM[7] 0	WM[6] 0	— 0	— 0	WM[5] 0	WM[4] 0	WM[3] 0	WM[2] 0	WM[1] 0	WM[0] 0	0000h
		204h	RAM write data mask (2)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	WM[17] 0	WM[16] 0	WM[15] 0	WM[14] 0	WM[13] 0	WM[12] 0	0000h
		205h~ 20Fh	Setting disabled	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
	Window address control system	210h	Horizontal RAM address start position	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	HSA[7] 0	HSA[6] 0	HSA[5] 0	HSA[4] 0	HSA[3] 0	HSA[2] 0	HSA[1] 0	HSA[0] 0	0000h
		211h	Horizontal RAM address end position	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	HEA[7] 1	HEA[6] 1	HEA[5] 1	HEA[4] 0	HEA[3] 1	HEA[2] 1	HEA[1] 1	HEA[0] 1	00EF
		212h	Vertical RAM address start position	— 0	— 0	— 0	— 0	— 0	— 0	— 0	VSA[8] 0	VSA[7] 0	VSA[6] 0	VSA[5] 0	VSA[4] 0	VSA[3] 0	VSA[2] 0	VSA[1] 0	VSA[0] 0	0000h
		213h	Vertical RAM address end position	— 0	— 0	— 0	— 0	— 0	— 0	— 0	VEA[8] 1	VEA[7] 0	VEA[6] 0	VEA[5] 1	VEA[4] 1	VEA[3] 1	VEA[2] 1	VEA[1] 1	VEA[0] 1	013Fh
		214h	Moving picture control address start position	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	EHSA[7] 0	EHSA[6] 0	EHSA[5] 0	EHSA[4] 0	EHSA[3] 0	EHSA[2] 0	EHSA[1] 0	EHSA[0] 0	0000h
		215h	Moving picture control address end position	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	EHEA[7] 1	EHEA[6] 1	EHEA[5] 1	EHEA[4] 0	EHEA[3] 1	EHEA[2] 1	EHEA[1] 1	EHEA[0] 1	00EFh
		216h	Moving picture control address start position	— 0	— 0	— 0	— 0	— 0	— 0	— 0	EVSA[8] 0	EVSA[7] 0	EVSA[6] 0	EVSA[5] 0	EVSA[4] 0	EVSA[3] 0	EVSA[2] 0	EVSA[1] 0	EVSA[0] 0	0000h
		217h	Moving picture control address end position	— 0	— 0	— 0	— 0	— 0	— 0	— 0	EVEA[8] 1	EVEA[7] 0	EVEA[6] 0	EVEA[5] 1	EVEA[4] 1	EVEA[3] 1	EVEA[2] 1	EVEA[1] 1	EVEA[0] 1	013Fh
		218h~ 2FFh	Setting disabled	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
3**	γ-control system	300h	γ-control (1)	— 0	PKP3[2] 0	PKP3[1] 1	PKP3[0] 0	— 0	PKP2[2] 0	PKP2[1] 0	PKP2[0] 1	— 0	PKP1[2] 0	PKP1[1] 1	PKP1[0] 1	— 0	PKP0[2] 0	PKP0[1] 1	PKP0[0] 0	2132h
		301h	γ-control (2)	— 0	PRP3[2] 0	PRP3[1] 1	PRP3[0] 0	— 0	PRP2[2] 0	PRP2[1] 0	PRP2[0] 1	— 0	PRP1[2] 1	PRP1[1] 0	PRP1[0] 0	— 0	PRP0[2] 0	PRP0[1] 0	PRP0[0] 1	2141h
		302h	γ-control (3)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	PRP4[2] 1	PRP4[1] 1	PRP4[0] 0	0006h
		303h	γ-control (4)	— 0	PRP8[2] 0	PRP8[1] 0	PRP8[0] 1	— 0	PRP7[2] 1	PRP7[1] 0	PRP7[0] 0	— 0	PRP6[2] 0	PRP6[1] 0	PRP6[0] 1	— 0	PRP5[2] 0	PRP5[1] 0	PRP5[0] 1	1411h
		304h	γ-control (5)	— 0	— 0	— 0	VRP1[4] 1	VRP1[3] 0	VRP1[2] 0	VRP1[1] 0	VRP1[0] 0	— 0	— 0	— 0	— 0	VRP0[3] 1	VRP0[2] 0	VRP0[1] 1	VRP0[0] 1	100Bh
		305h	γ-control (6)	— 0	PKN3[2] 0	PKN3[1] 1	PKN3[0] 0	— 0	PKN2[2] 0	PKN2[1] 0	PKN2[0] 1	— 0	PKN1[2] 0	PKN1[1] 1	PKN1[0] 1	— 0	PKN0[2] 0	PKN0[1] 1	PKN0[0] 0	2132h
		306h	γ-control (7)	— 0	PRN3[2] 0	PRN3[1] 1	PRN3[0] 0	— 0	PRN2[2] 0	PRN2[1] 1	PRN2[0] 0	— 0	PRN1[2] 1	PRN1[1] 0	PRN1[0] 0	— 0	PRN0[2] 0	PRN0[1] 1	PRN0[0] 0	2242h
		307h	γ-control (8)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	PRN4[2] 1	PRN4[1] 1	PRN4[0] 0	0006h
		308h	γ-control (9)	— 0	PRN8[2] 0	PRN8[1] 1	PRN8[0] 1	— 0	PRN7[2] 1	PRN7[1] 0	PRN7[0] 0	— 0	PRN6[2] 0	PRN6[1] 1	PRN6[0] 0	— 0	PRN5[2] 0	PRN5[1] 0	PRN5[0] 1	3421h
		309h	γ-control (10)	— 0	— 0	— 0	VRN1[4] 0	VRN1[3] 1	VRN1[2] 0	VRN1[1] 1	VRN1[0] 1	— 0	— 0	— 0	— 0	VRN0[3] 0	VRN0[2] 1	VRN0[1] 1	VRN0[0] 1	0B07h
		310h~ 3FFh	Setting disabled	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
4**	Coordinate control system	400h	Line number control	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	NL[5] 1	NL[4] 0	NL[3] 0	NL[2] 1	NL[1] 1	NL[0] 1	0027h
		401h	Screen control	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	— 0	VLE 0	REV 0	0000h
		402h	Full screen image RAM area (Start line)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	BSA[8] 0	BSA[7] 0	BSA[6] 0	BSA[5] 0	BSA[4] 0	BSA[3] 0	BSA[2] 0	BSA[1] 0	BSA[0] 0	0000h
		403h	Full screen image RAM area (End line)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	BEA[8] 1	BEA[7] 0	BEA[6] 0	BEA[5] 1	BEA[4] 1	BEA[3] 1	BEA[2] 1	BEA[1] 1	BEA[0] 1	013Fh
		404h	vertical scroll control	— 0	— 0	— 0	— 0	— 0	— 0	— 0	VL[8] 0	VL[7] 0	VL[6] 0	VL[5] 0	VL[4] 0	VL[3] 0	VL[2] 0	VL[1] 0	VL[0] 0	0000h
		405h~ 4FFh	Setting disabled	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
5**	Partial display control system	500h	Partial image 1 display position	— 0	— 0	— 0	— 0	— 0	— 0	— 0	PTDP0[8] 0	PTDP0[7] 0	PTDP0[6] 0	PTDP0[5] 0	PTDP0[4] 0	PTDP0[3] 0	PTDP0[2] 0	PTDP0[1] 0	PTDP0[0] 0	0000h
		501h	Partial image 1 RAM area (Start line)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	PTSA0[8] 0	PTSA0[7] 0	PTSA0[6] 0	PTSA0[5] 0	PTSA0[4] 0	PTSA0[3] 0	PTSA0[2] 0	PTSA0[1] 0	PTSA0[0] 0	0000h
		502h	Partial image 1 RAM area (End line)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	PTEA0[8] 0	PTEA0[7] 0	PTEA0[6] 0	PTEA0[5] 0	PTEA0[4] 0	PTEA0[3] 0	PTEA0[2] 0	PTEA0[1] 0	PTEA0[0] 0	0000h
		503h	Partial image 2 display position	— 0	— 0	— 0	— 0	— 0	— 0	— 0	PTDP1[8] 0	PTDP1[7] 0	PTDP1[6] 0	PTDP1[5] 0	PTDP1[4] 0	PTDP1[3] 0	PTDP1[2] 0	PTDP1[1] 0	PTDP1[0] 0	0000h
		504h	Partial image 2 RAM area (Start line)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	PTSA1[8] 0	PTSA1[7] 0	PTSA1[6] 0	PTSA1[5] 0	PTSA1[4] 0	PTSA1[3] 0	PTSA1[2] 0	PTSA1[1] 0	PTSA1[0] 0	0000h
		505h	Partial image 2 RAM area (End line)	— 0	— 0	— 0	— 0	— 0	— 0	— 0	PTEA1[8] 0	PTEA1[7] 0	PTEA1[6] 0	PTEA1[5] 0	PTEA1[4] 0	PTEA1[3] 0	PTEA1[2] 0	PTEA1[1] 0	PTEA1[0] 0	0000h
		506h~ 5FFh	Setting disabled	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	

Note) Do not access an index where setting is not assigned.

Reset Function

■ **Reset function**

The BD663474 is internally initialized by entering “Low” level from the RESET* terminal.
The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the CR oscillation frequency stabilizes after power is supplied (10 ms). During this period, do not access the RAM or make any initial instruction setting.

Initial state of instruction register after reset

(1) All the inside registers are initialized. The default value of each instruction bit is shown in the instruction list. Refer to the figure shown in the lower space for the respective instruction bit in the list.

Initial state of internal RAM data after reset

(1) The internal RAM data is not initialized by the reset function. After powering on, initialize the RAM data during a display-off period (D1-0 = “00”). If reset is done without turning the power off, the RAM data written immediately before the reset is retained.

Reset input during deep standby mode

(1) Oscillator starts operating.
(2) The states of output terminals are as follows.
DDVDH, VGH = PVcc VGL, VCL = GND VciOUT = GND VDCDC2 = DDVDH
Vcom = GND VcomH=GND VcomL=GND VDH = GND
S1-S720=GND G1–G320 = VGH

Reset input during deep standby mode

If a RESET input enters the BD663474 during deep standby mode, the inside logic and regulator start the transition to the initial state, which may leave the state of interface pins unstable during this period. For this reason, do not enter a RESET input during deep standby mode.

System Interfaces

The following system interfaces are available with the BD663474 by setting the IM3/2/1/0 pins.
The system interface is used for instruction setting and RAM access.

IM3	IM2	IM1	IM0	System interface	DP pin	Available colors	Note
0	0	0	0	Setting disabled	–	–	
0	0	0	1	Setting disabled	–	–	
0	0	1	0	80-series 18-bit interface	DB17-10, 8-1	65,536 colors (262,144 colors)	1
0	0	1	1	80-series 8-bit interface (Big-endien)	DB17-10	65,536 colors (262,144 colors)	2
0	1	0	ID	Serial peripheral interface (SPI)	SDI, SDO	65,536 colors	
0	1	1	0	Setting disabled	–	–	
0	1	1	1	80-series 8-bit interface (Little-endien)	DB17-10	65,536 colors (262,144 colors)	2
1	0	0	0	Setting disabled	–	–	
1	0	0	1	Setting disabled	–	–	
1	0	1	0	80-series 18-bit interface	DB17-0	262,144 colors	
1	0	1	1	80-series 9-bit interface	DB17-9	262,144 colors	
1	1	0	ID	Serial peripheral interface (SPI) (When SDO non-output: Hi-Z)	SDI, SDO	65,536 colors	
1	1	1	*	Setting disabled	–	–	

Note 1: Maximum 262,144 colors available in 2-transfer mode.
Note 2: Maximum 262,144 colors available in 3-transfer mode.

(1) 80-series 18-bit bus interface

80-series 18-bit parallel data is transferred by setting the IM3/2/1/0 pins to Vcc1/GND/Vcc1/GND levels.

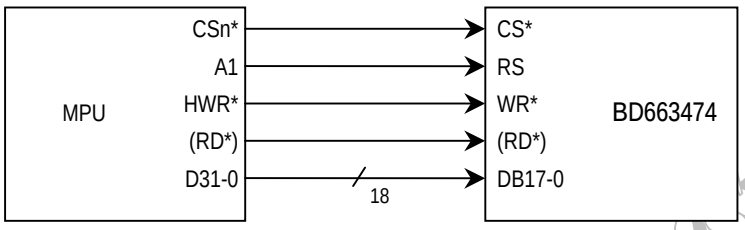
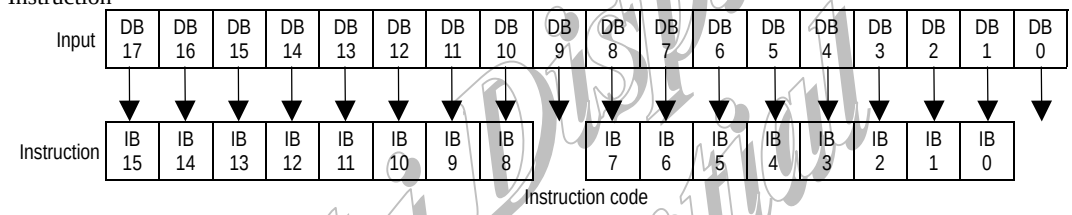


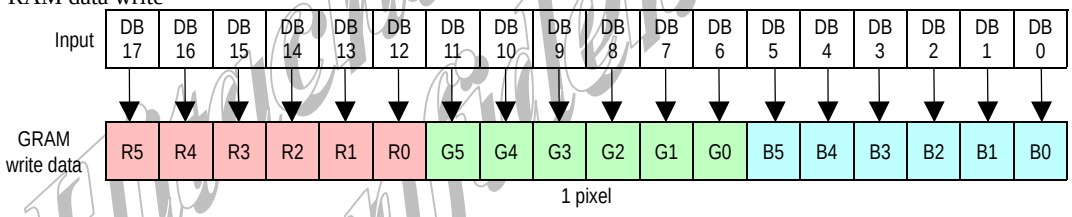
Diagram: Example of interface with 32-bit microcomputer

[18-bit interface data format]

- Instruction



- RAM data write



* 262,144 colors are available in 18-bit system interface mode.

(2) 80-series 16-bit bus interface

80-series 16-bit parallel data is transferred by setting the IM3/2/1/0 pins to Vcc1/GND/Vcc1/GND levels. Fix unused pins DB9 and DB0 to either the IOVcc or GND level.

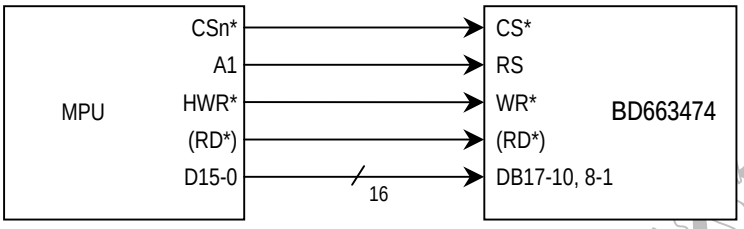
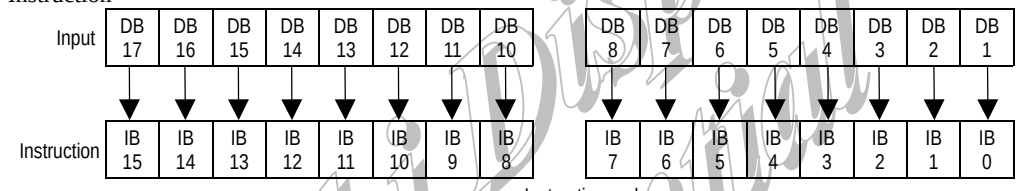


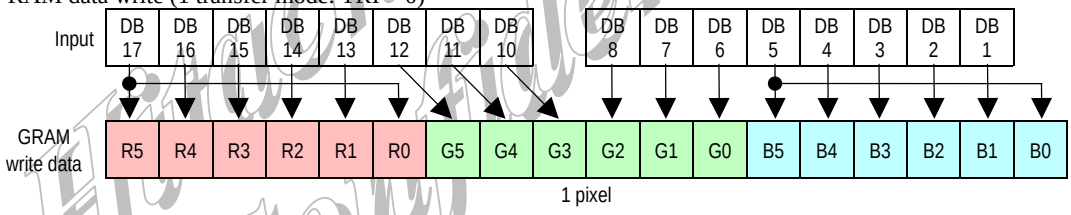
Diagram: Example of interface with 16-bit microcomputer

[16-bit interface data format]

- Instruction

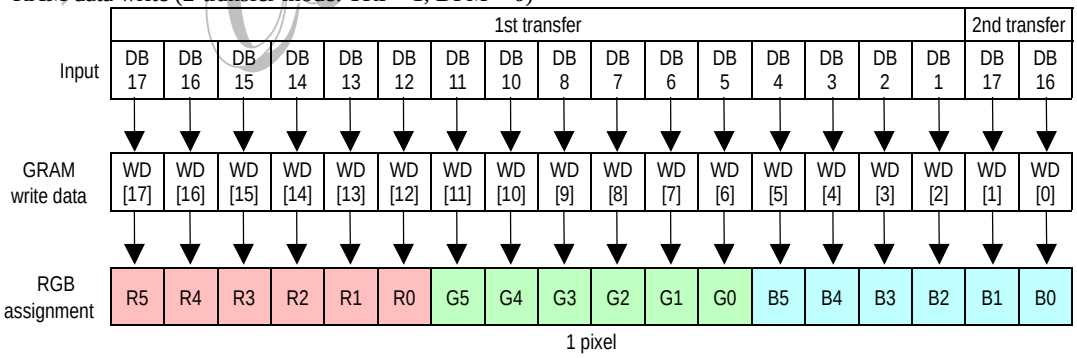


- RAM data write (1 transfer mode: TRI = 0)



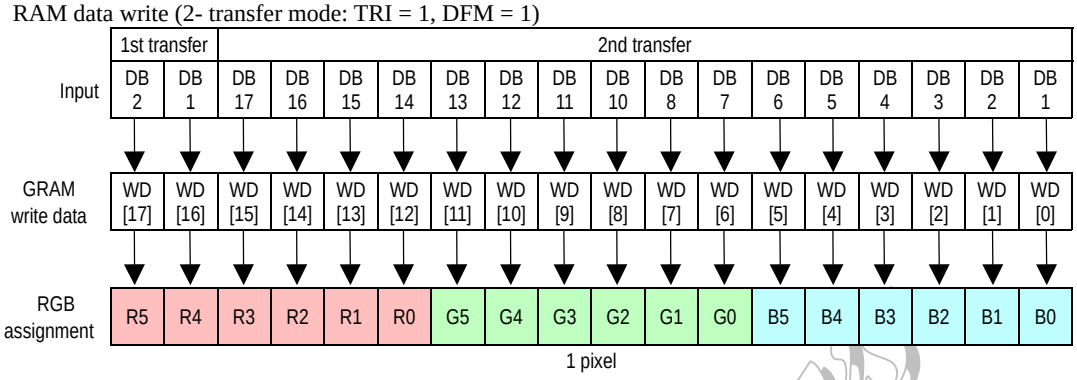
* 65,536 colors are available in 16-bit system interface 1-transfer mode.

- RAM data write (2-transfer mode: TRI = 1, DFM = 0)



* 262,144 colors are available in 16-bit system interface 2-transfer mode.

- RAM data write (2- transfer mode: TRI = 1, DFM = 1)



* 262,144 colors are available in 16-bit system interface 2-transfer mode.

Note : Data transfer synchronization in 16-bit × 2-transfer bus interface mode.

The BD663474 supports a data transfer synchronization function, which forcibly resets the counters that count the data transfer of the upper 16 and lower two bits, or upper two and lower 16 bits in 16-bit × 2-transfer mode. If a mismatch occurs in data transfer due to noise and so on, the "000H" instruction is written four times to reset the upper and lower counters, and so data transfer restarts from the upper bits. This synchronization function, when executed periodically, prevents the runaway of the display system.

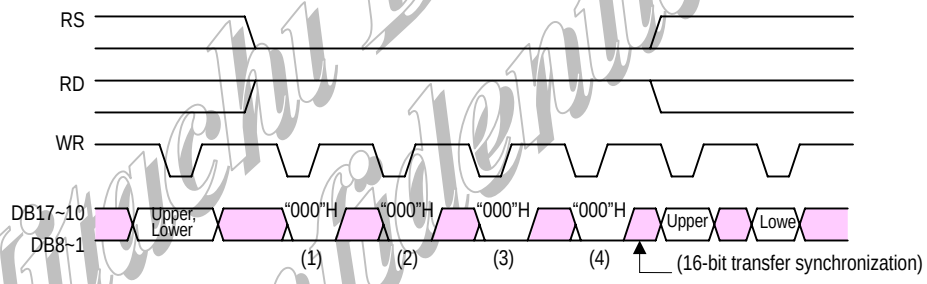


Diagram: 16-bit data transfer synchronization

(3) 80-series 9-bit bus interface

80-series 9-bit parallel data is transferred through the DB17-9 pins by setting the IM3/2/1/0 pins to Vcc1/GND/Vcc1/Vcc1 levels. When a 16-bit instruction is transferred, the data is divided into the upper and lower eight bits (the least significant single bit is not used), and the upper eight bits are transferred first. The RAM data is also divided into the upper and lower nine bits, and the upper nine bits are transferred first. The unused DB8-0 pins must be fixed to either the IOVcc or GND level.

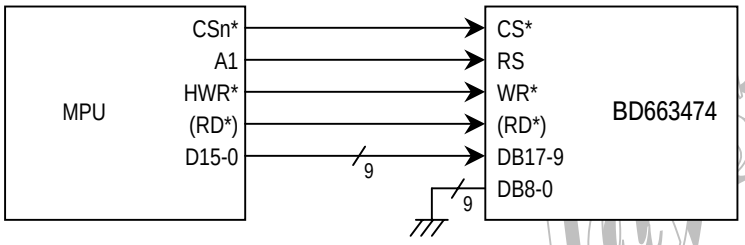
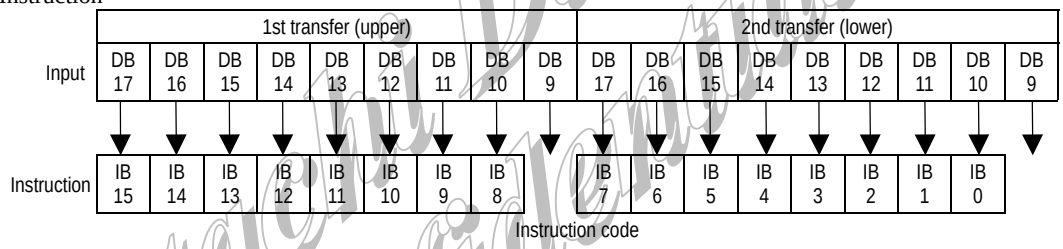


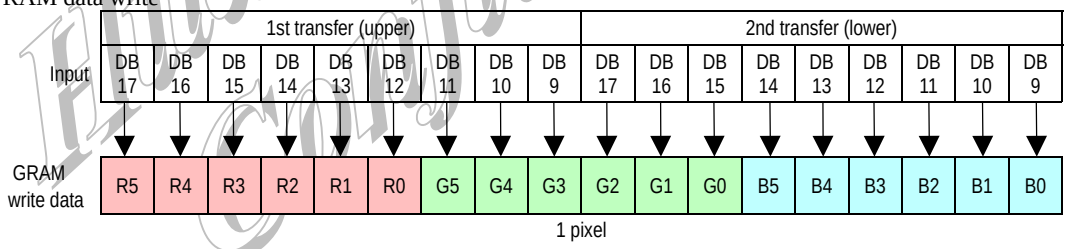
Diagram: Example of interface with 16-bit microcomputer

[16-bit interface data format]

- Instruction



- RAM data write



* 262,144 colors are available in 9-bit system interface mode.

Note : Data transfer synchronization in 9-bit × 2-transfer bus interface mode.

The BD663474 supports a data transfer synchronization function, which forcibly resets the counters that count the data transfer of upper lower bits in 9-bit bus interface mode. If a mismatch occurs in data transfer of the upper and lower nine bits due to noise and so on, the "000H" instruction is written four times consecutively to reset the upper and lower counters, and so data transfer restarts from the upper bits. This synchronization function, when executed periodically, prevents the runaway of the display system.

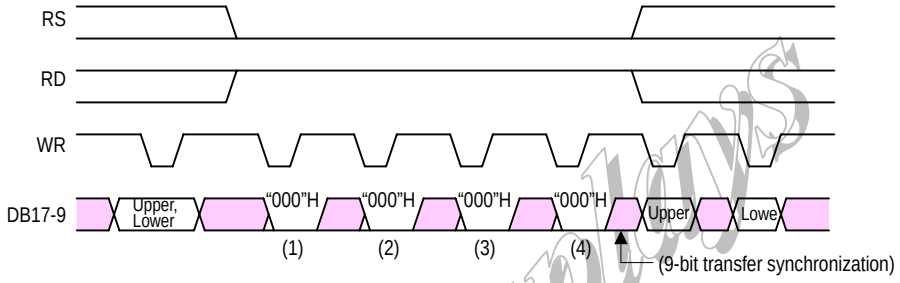


Diagram: 9-bit data transfer synchronization

(4) 80-series 8-bit bus interface (Big-endien)

80-series 8-bit parallel data is transferred through the DB17-10 pins by setting the IM3/2/1/0 pins to GND/GND/Vcc1/Vcc1 levels. When transferring a 16-bit instruction, data is divided into the upper and lower eight bits, and the upper eight bits are transferred first. The RAM data is also divided into the upper and lower eight bits, and the upper eight bits are transferred first. The RAM write data is expanded into 18 bits internally as follows. The unused DB9-0 pins must be fixed to either the IOVcc or GND level.

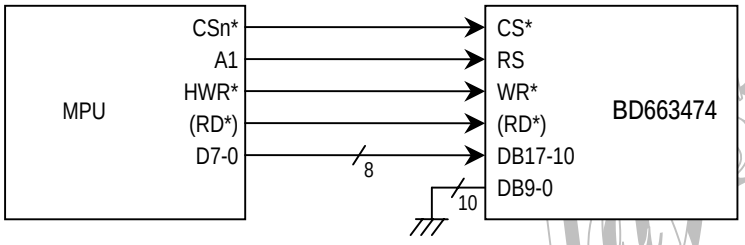
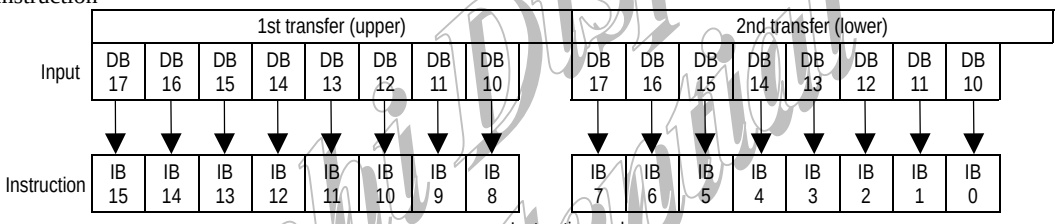


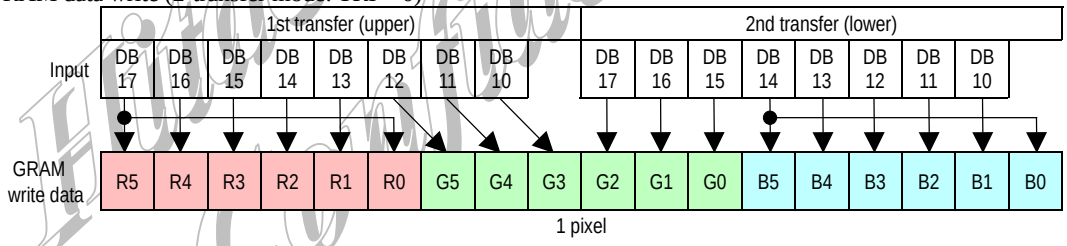
Diagram: Example of interface with 8-bit microcomputer

[8-bit interface data format]

- Instruction

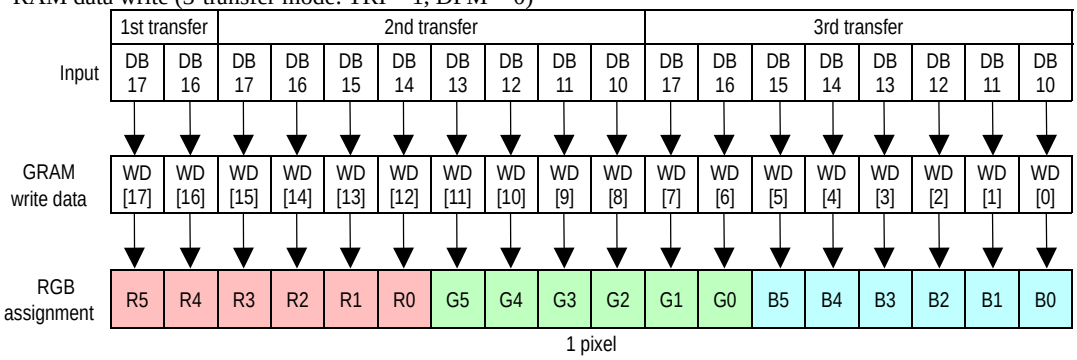


- RAM data write (2-transfer mode: TRI = 0)



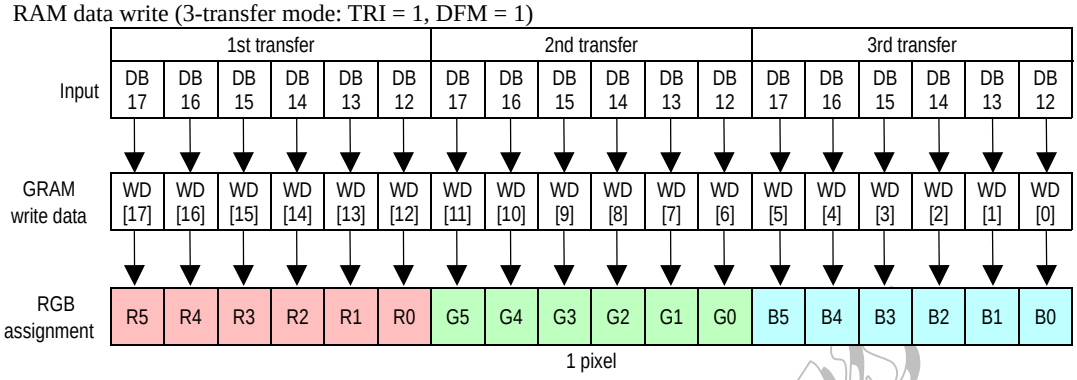
* 65,536 colors are available in 8-bit system interface 2-transfer mode.

- RAM data write (3-transfer mode: TRI = 1, DFM = 0)



* 262,144 colors are available in 8-bit system interface 3-transfer mode.

- RAM data write (3-transfer mode: TRI = 1, DFM = 1)



* 262,144 colors are available in 8-bit system interface 3-transfer mode.

Note : Data transfer synchronization in 8-bit × 2-transfer bus interface mode.

The BD663474 supports a data transfer synchronization function, which forcibly resets the counters that count the data transfer of the upper lower bits in the 8-bit bus interface mode. If a mismatch occurs in data transfer of the upper and lower eight bits due to noise and so on, the "000H" instruction is written four times consecutively to reset the upper and lower counters, and so data transfer restarts from the upper bits. This synchronization function, when executed periodically, prevents the runaway of the display system.

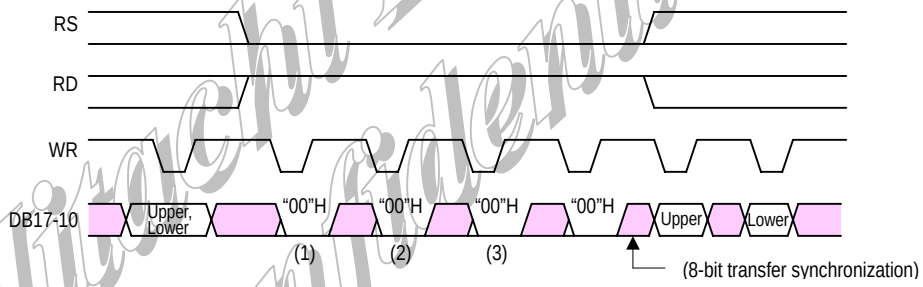


Diagram: 8-bit data transfer synchronization

(5) Serial peripheral interface (SPI)

A serial peripheral interface (SPI) is selected by setting the IM3/2/1 pins to the GND/Vcc1/GND levels or Vcc1/Vcc1/GND levels. This interface is available through four lines: the chip select (CS), serial transfer clock (SCL), serial input data (SDI), and serial output data (SDO). The DB17-0 pins, which are not used during this mode, must be fixed to either the IOVcc or GND level.

The BD663474 recognizes the start of data transfer on the falling edge of CS input to initiate the transfer of the start-byte. It recognizes the end of data transfer on the rising edge of CS input. When the IM3/2/1 pins are set to Vcc1/Vcc1/GND levels, SDO output becomes Hi-Z during the period of CS input = "1" (i.e. the period when the BD663474 is not selected) and the SDO line can be shared with other chips.

In the chip select procedure of the BD663474, the chip address (six bits) in the start-byte sent from a sending end and the device ID code (six bits) assigned to the BD663474 are compared first. When the two correspond, the BD663474 starts taking in subsequent data. The least significant bit of the device ID code is set by the ID pin. Send "01110" to the five upper bits of the device ID code. Two different chip addresses must be assigned to the BD663474 because the seventh bit of the start byte is assigned to the RS (register select) of the BD663474. When RS = 0, either an index register write operation or a status read operation is executed. When RS = 1, either an instruction write operation or a RAM read/write operation is executed. The eighth bit of the start byte is for the RW bit of the BD663474. Data is received when the RW bit = 0. Data is transmitted when the RW bit = 1.

In SPI mode, data is written to the GRAM after transferring two bytes. Data is expanded into 18 bits before being written to the GRAM by adding one bit to the least significant bit of the R and B data. The same data as the most significant bits of R and B data is written.

After receiving the start byte, the BD663474 starts transmitting or receiving data in units of bytes. Data transfer is executed from the most significant bit (MSB). All instructions of the BD663474 take a 16-bit format and are executed internally from the MSB after transferring two bytes (DB15-0). RAM write data is internally expanded to 18 bits.
After receiving a start byte, the BD663474 takes in the upper eight bits of the instruction as the first byte, and the lower eight bits as the second byte. The 5-byte data read out from the RAM immediately after the start byte is invalid. Valid data is read out from the sixth byte.

Table: Start byte format

Example of transferred bit	S	1	2	3	4	5	6	7	8
Start byte format	Start	0	1	1	1	0	ID	RS	R/W

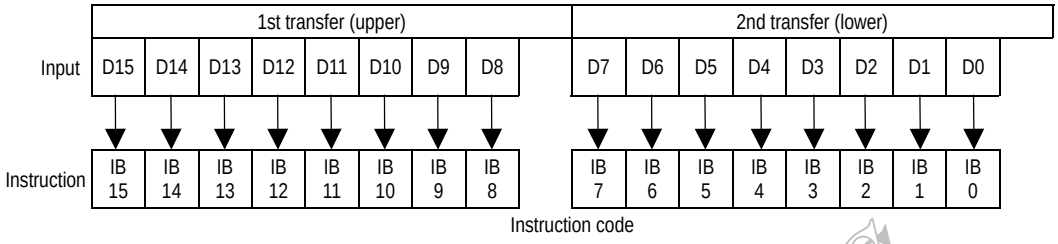
Note: ID bit is selected by setting IM0/ID pins

Table: RS, R/W bit function

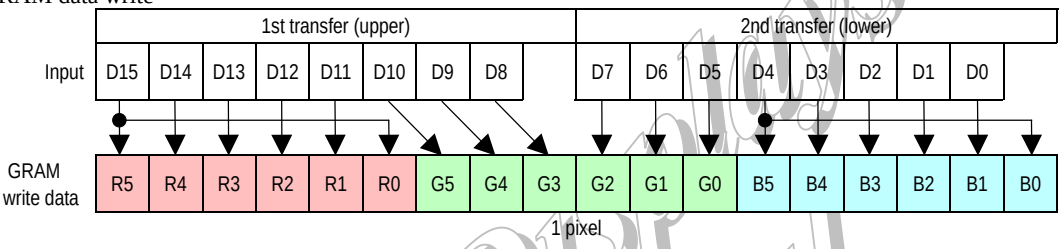
RS	R/W	Function
0	0	Sets index register
0	1	Reads status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

[Serial peripheral interface data format]

- Instructions



- RAM data write



* 65,536 colors are available in serial peripheral interface mode.

a) Basic data transfer through serial peripheral interface.

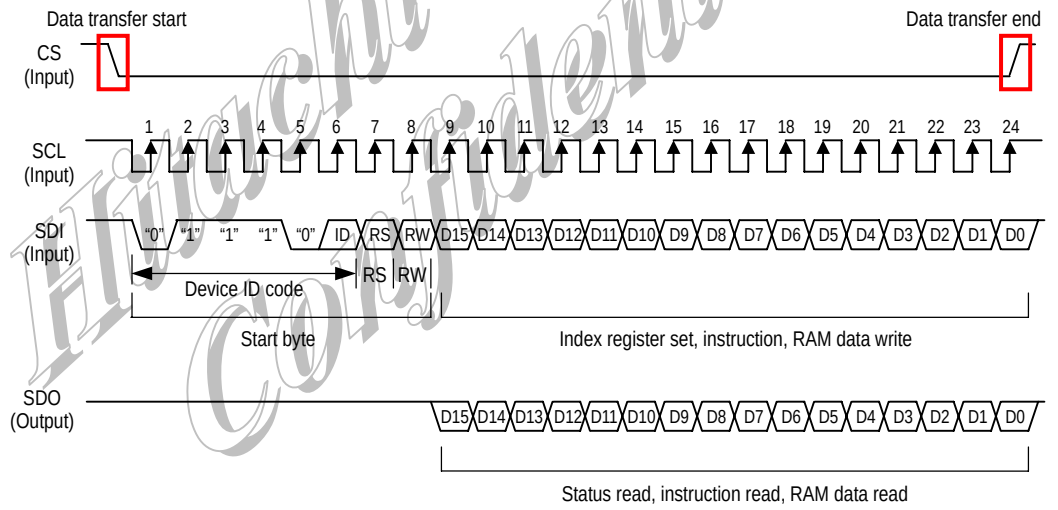
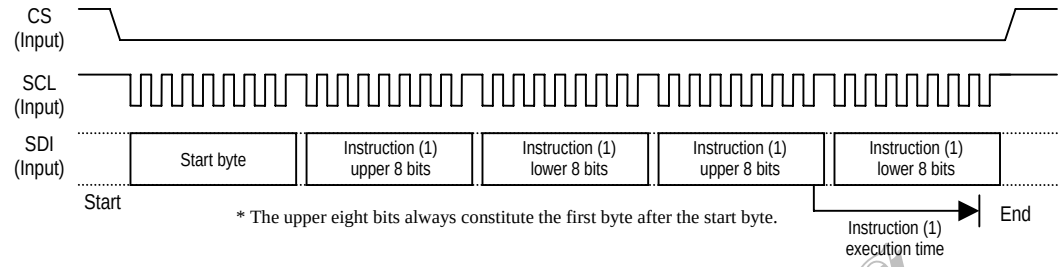
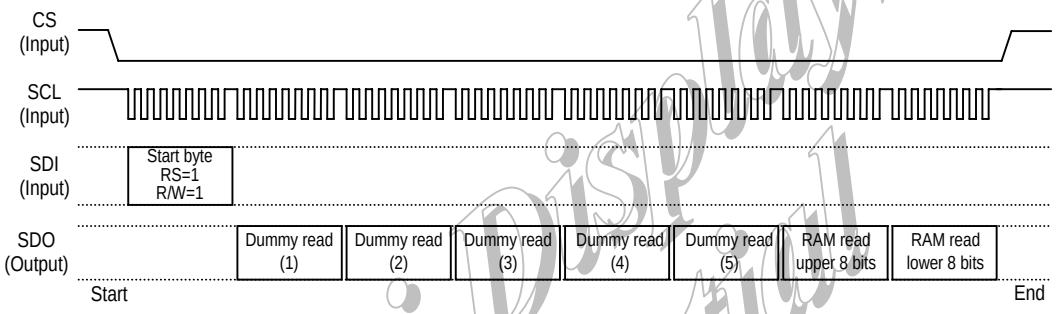


Diagram: Data transfer timing for serial peripheral interface (1)

b) Consecutive data transfer through serial peripheral interface.



c) RAM data read transfer



d) Status read / Instruction read

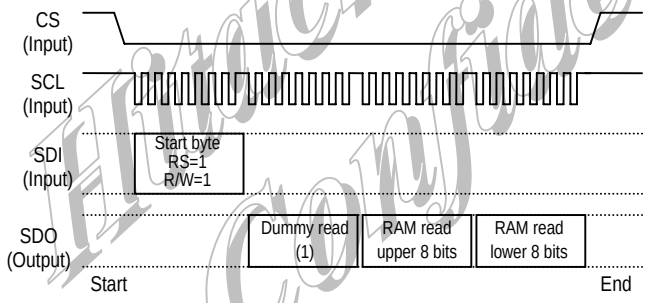


Diagram: Data transfer timing for serial peripheral interface (2)

(6) 80-series 8-bit bus interface (Little-endien)

80-series 8-bit parallel data is transferred through the DB17-10 pins by setting the IM3/2/1/0 pins to GND/GND/Vcc1/Vcc1 levels. When transferring a 16-bit instruction, data is divided into the upper and lower eight bits, and the lower eight bits are transferred first. The RAM data is also divided into the upper and lower eight bits, and the lower eight bits are transferred first. The RAM write data is expanded into 18 bits internally as follows. The unused DB9-0 pins must be fixed to either the IOVcc or GND level.

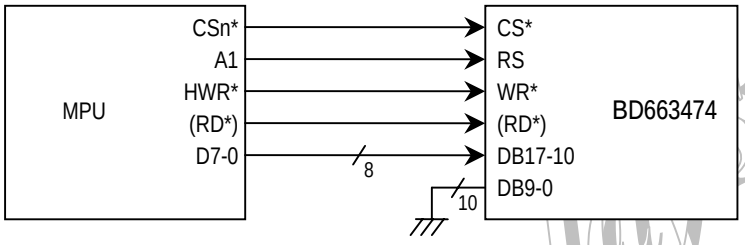
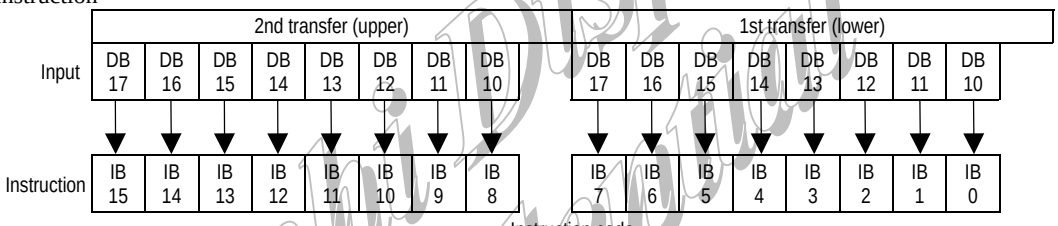


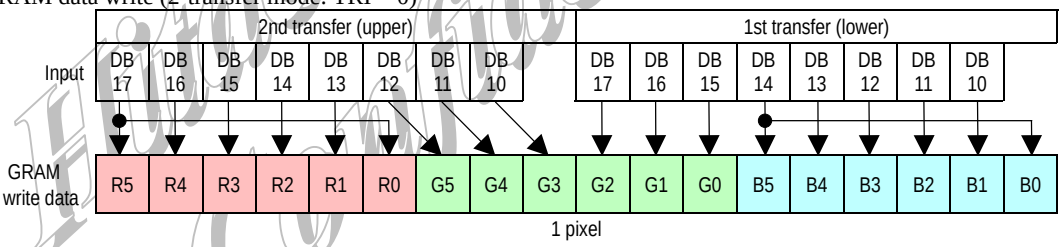
Diagram: Example of interface with 8-bit microcomputer

[8-bit interface data format]

- Instruction



- RAM data write (2-transfer mode: TRI = 0)



* 65,536 colors are available in 8-bit system interface 2-transfer mode.

Note : Data transfer synchronization in 8-bit × 2-transfer bus interface mode.

The BD663474 supports a data transfer synchronization function, which forcibly resets the counters that count the data transfer of the upper lower bits in 8-bit bus interface mode. If a mismatch occurs in the data transfer of the upper and lower eight bits due to noise and so on, the “000H” instruction is written four times consecutively to reset the upper and lower counters, and so data transfer restarts from the lower bits. This synchronization function, when executed periodically, prevents the runaway of the display system.

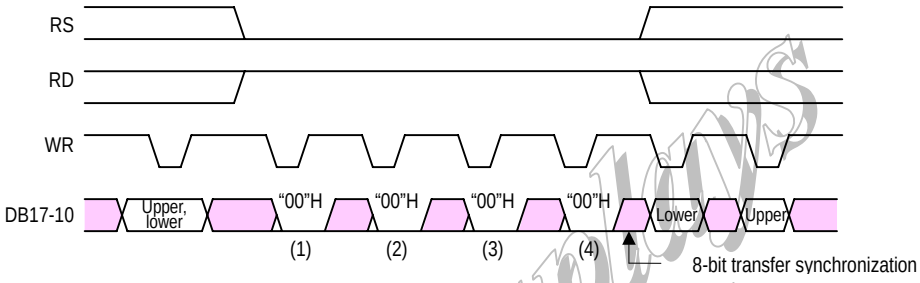


Diagram: 8-bit data transfer synchronization

RAM Address and Display Position on Panel

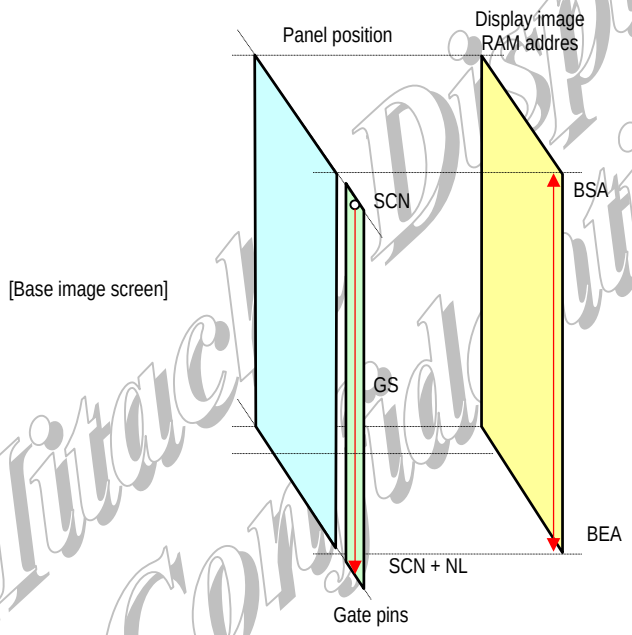
The BD663474 has a memory of 240RGB × 320-line display data, which enables display on a QVGA-size panel (240RGB×320 lines).

The BD663474 enables the display of various images by the following settings.

(1) Specify the RAM areas (BSA, BEA) for the graphics displayed on the base image screen.
(2) Specify the display start positions (PTDPx) for the first and second screens in partial display mode.
(3) Specify the gate terminals (SCN, NL) to drive the base image screen and its scan sequence (GS).
(4) After display ON, set the enable bits (BASEE, PTDE) for each image.

Note: To switch the display position in the horizontal direction, the SS bit must be set when writing data in the RAM.

[Pattern diagrams for RAM address, display position, and driving position]



- **Restrictions on setting display control register**

Note the following restrictions on setting the coordinates of display data, display positions, and partial display.

(1) Display screen setting

1. The following relations must be observed:
   - NL ≤ 320 lines
   - 0 ≤ SCN < SCN + NL ≤ 320 lines

(2) Normal display setting

1. The image starts to be displayed at the first line of each screen.
2. Set the RAM area of the display image (BSA, BEA) so that the number of lines to be displayed on the screen is equal to or more than the number of lines to drive the entire panel (NL).
   - BEA – BSA ≥ NL
3. The relation between BSA and BEA (display image RAM area) must be as follows:
   - BEA > BSA

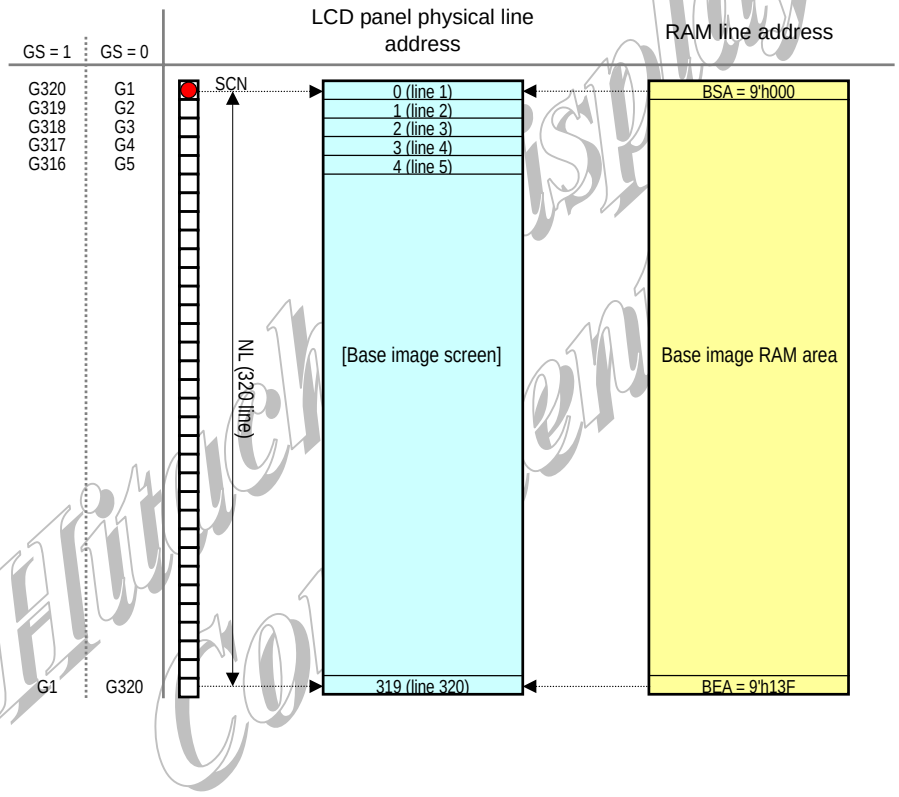
(3) Partial display setting

1. The display start position must be PTDP0[8:0] ≥ 9'h000, PTDP1[8:0] ≥ 9'h000.
2. The image starts to be displayed at the lines specified below.
   - Display start position of first screen: SCN + PTDP0 = PTSA0
   - Display start position of second screen: SCN + PTDP1 = PTSA1
3. Set the RAM area of the display image (BSA, BEA) as follows. The partial display is available in the (BSA, BEA) specified area.
   - BEA – BSA ≤ NL – PTDP0
   - BEA – BSA ≤ NL – PTDP1
4. The relation between BSA and BEA (display image RAM area) must be as follows:
   - BEA > BSA

- **Example of instruction setting (1)**

  - Normal display on QVGA-size panel: 240RGB × 320 lines

Instructions for base image screen	
NL [5:0]	6'h27
SCN [5:0]	6'h00
BASEE	1'h1
BSA [8:0]	9'h000
BEA [8:0]	9'h13F

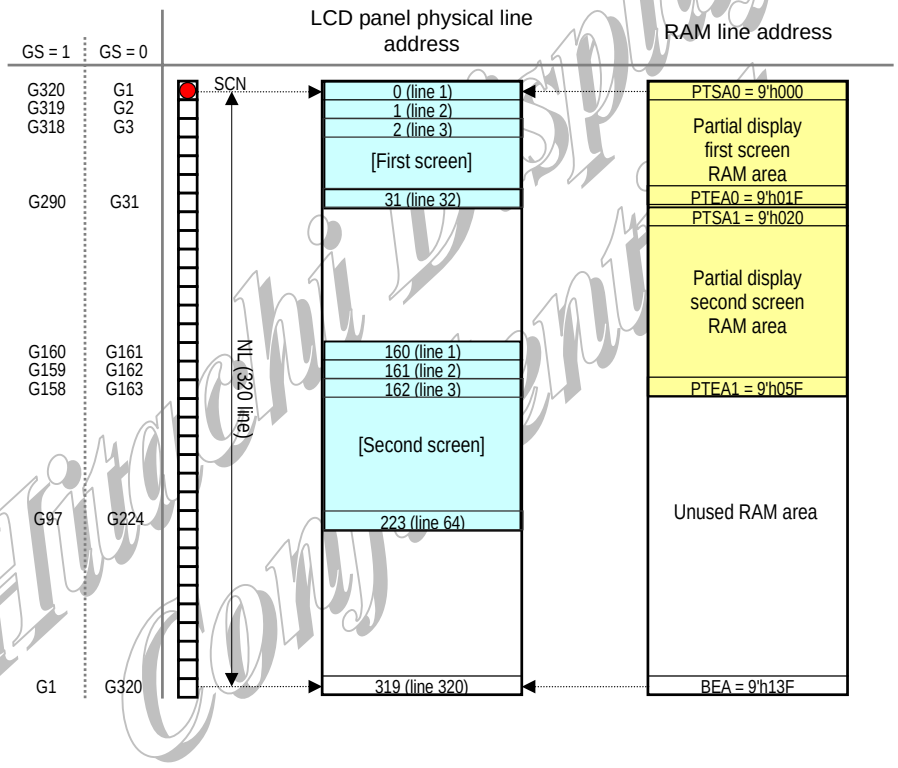


- **Example of instruction setting (2)**

Partial display (first screen): 240RGB × 32 lines
Partial display (second screen): 240RGB × 64 lines

Instructions for first screen	
NL [5:0]	6'h1B
SCN [5:0]	6'h00
PTDE [0]	1'h1
PTDP0 [8:0]	9'h000
PTSA0 [8:0]	9'h000
PTEA0 [8:0]	9'h01F

Instructions for second screen	
-	-
-	-
PTDE [1]	1'h1
PTDP1 [8:0]	9'h0A0
PTSA1 [8:0]	9'h020
PTEA1 [8:0]	9'h05F



Resizing Function

The BD663474 has a resizing function which allows you to reduce images by ×1/2 and ×1/4 in horizontal and vertical directions when writing image data.

■ Contraction

(1) Description

The BD663474 has a function for writing the data of resized images into the RAM when the original image data is transferred through the window address function and the RSR bit representing the contraction rate of the image.

This function allows the system to just transfer the original image data as usual even if resizing is required, facilitating all kinds of displays such as resized camera images and thumbnails.

Note: The BD663474 processes contraction of an image simply by thinning out pixels. For this reason, resized images may seem distorted compared with the originals. Check the resized image before use.

Original image data

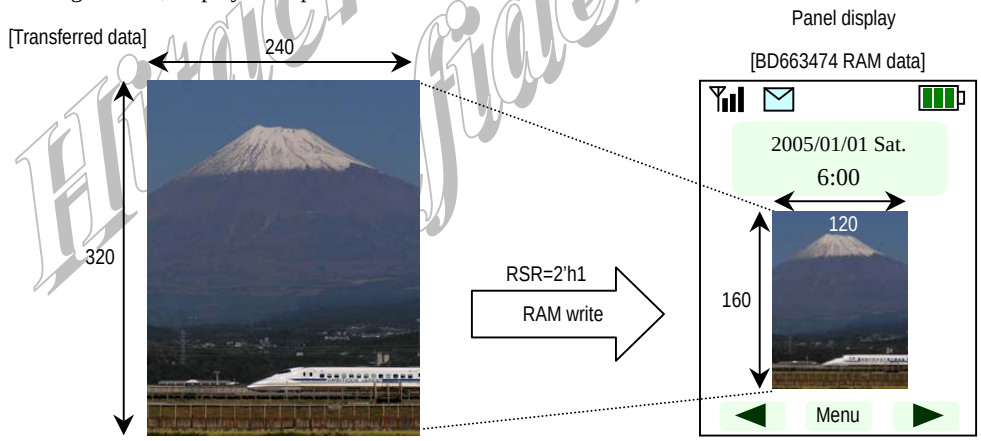
	0	1	2	3	4	5	6
0	(0, 0)	(0, 1)	(0, 2)	(0, 3)	(0, 4)	(0, 1)	(0, 1)
1	(1, 0)	(1, 1)	(1, 2)	(1, 3)	(1, 4)	(1, 1)	(1, 1)
2	(2, 0)	(2, 1)	(2, 2)	(2, 3)	(2, 4)	(2, 1)	(2, 1)
3	(3, 0)	(3, 1)	(3, 2)	(3, 3)	(3, 4)	(3, 1)	(3, 1)
4	(4, 0)	(4, 1)	(4, 2)	(4, 3)	(4, 4)	(4, 1)	(4, 1)
5	(5, 0)	(5, 1)	(5, 2)	(5, 3)	(5, 4)	(5, 1)	(5, 1)
6	(6, 0)	(6, 1)	(6, 2)	(6, 3)	(6, 4)	(6, 1)	(6, 1)

1/2 resizing

RAM data

	0	1	2	3
0	(0, 0)	(0, 1)	(0, 2)	(0, 3)
1	(1, 0)	(1, 1)	(1, 2)	(1, 3)
2	(2, 0)	(2, 1)	(2, 2)	(2, 3)
3	(3, 0)	(3, 1)	(3, 2)	(3, 3)

- Resizing transfer, display example

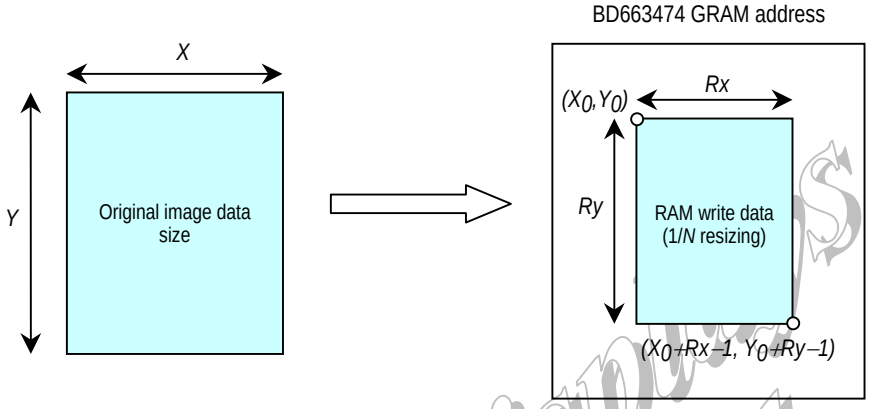


- Size of displayed image after resizing (for reference)

Original image size	Resized image size	
(X × Y)	1/2 (RSR = 2'h1)	1/4 (RSR = 2'h3)
640 × 480 (VGA)	320 × 240	160 × 120
350 × 288 (CIF)	176 × 144	88 × 72
320 × 240 (QVGA)	160 × 120	80 × 60
176 × 144 (QCIF)	88 × 72	44 × 36
120 × 160	60 × 80	30 × 40
132 × 176	66 × 88	32 × 44

(2) Resizing setting

In the BD663474, the RSR bit sets the resizing rate. The window addresses must be set so that the RAM window address area fits the size of the picture after resizing. If resizing creates surplus pixels, which are calculated from the equations below, set them in the RCV and RCH registers before writing data to the RAM



[Formulae for calculating the number of surplus pixels]

Number of surplus pixels in horizontal direction: $L = X \bmod N$

Number of surplus pixels in vertical direction: $M = Y \bmod N$

Resized picture size in horizontal direction: $Rx = (X - L)/N$

Resized picture size in vertical direction: $Ry = (Y - M)/N$

Original image (before resizing)	
Number of data in horizontal direction	X
Number of data in vertical direction	Y
Resizing ratio	1/N
	(N = 2, 4)

BD663474 setting		
Resizing setting	**RSR**	**N – 1**
Number of surplus pixels in vertical direction	RCV	L
Number of surplus pixels in horizontal direction	RCH	M
RAM writing start address	AD	(X_0, Y_0)
RAM window address	HSA	X_0
	HEA	$X_0 + Rx - 1$
	VSA	Y_0
	VEA	$Y_0 + Ry - 1$

(3) Resizing instructions

Setting for resizing ratio

RSR [1:0]	Resizing ratio
2'h0	No resizing (×1)
2'h1	×1/2
2'h2	Setting disabled
2'h3	×1/4

Setting for surplus pixels in vertical direction

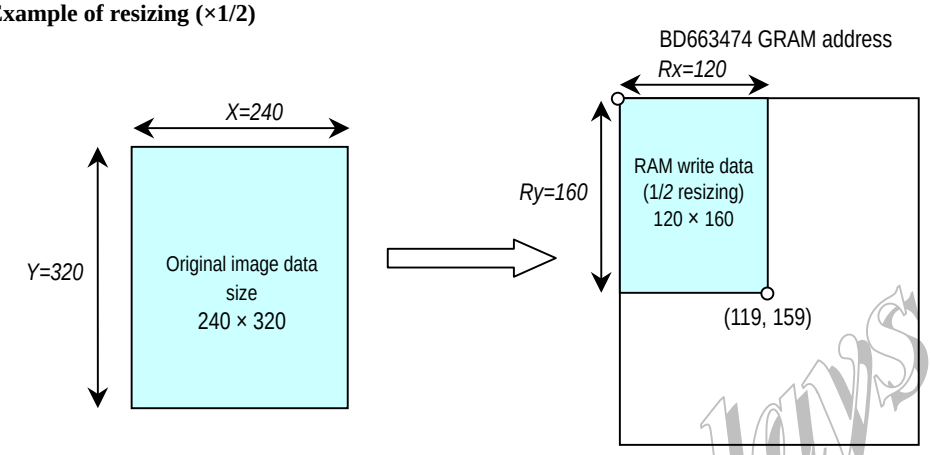
RCV [1:0]	Number of surplus pixels in vertical direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixel
2'h3	3 pixel

Setting for surplus pixels in horizontal direction

RCH [1:0]	Number of surplus pixels in horizontal direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixel
2'h3	3 pixel

* 1 pixel = 1 RGB

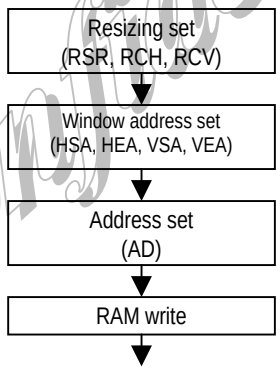
(4) Example of resizing (×1/2)



Original image (before resizing)		
Number of data in horizontal direction	X	240
Number of data in vertical direction	*Y*	320
Resizing ratio	1/*N*	1/2

BD663474 setting		
Resizing setting	RSR	2'h1
Number of surplus pixels in vertical direction	RCV	2'h0
Number of surplus pixels in horizontal direction	RCH	2'h0
RAM writing start address	AD	17'h00000
RAM window address	HSA	9'h00
	HEA	9'h77
	VSA	9'h00
	VEA	9'h9F

(5) RAM-write sequence of resized image



(6) Notes on using resizing function

(a) Set the resizing instruction (RSR, RCH, RCV) before writing data to the RAM.

(b) When writing data to the RAM using the resizing function, always start writing data from the first address of the window address area in units of lines.

(c) Set the window address area to fit the size of the resized image.

(d) Set the addresses before starting to transfer and write the data to the RAM.

(e) Set the RCH and RCV registers only when using the resizing function. When not using the resizing function (when RSR = 2'h0), set RCH = RCV = 2'h0.

External Display Interface

VSYNC Interface

Display Synchronous Data Transfer

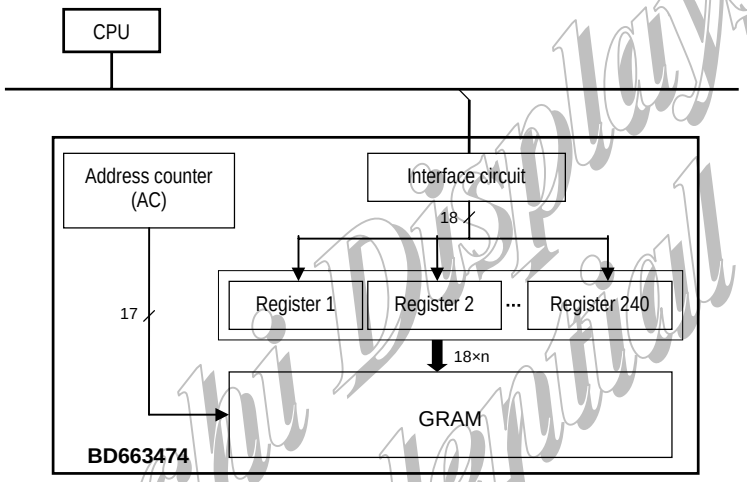
LC Panel Interface Timing

High-Speed RAM Write Mode

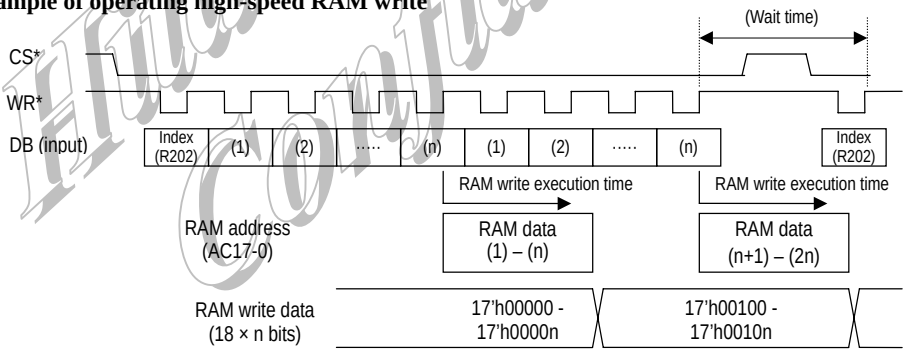
■ **Description**

The BD663474 has a high-speed RAM write function. This function makes the BD663474 compliant with applications that require high-speed rewriting of display data for displaying colored moving pictures.

In high-speed RAM write mode (HWM = 1), data is first latched in the internal write register of the BD663474 before being written to each horizontal line specified by the window address. Since the data latched in the internal register is transferred to the internal RAM collectively, it is possible to transfer data to the RAM while writing the next data to the write register. This operation can minimize the frequency of RAM access and enables consecutive RAM access with less power consumption.



■ **Example of operating high-speed RAM write**



■ **Notes on using high-speed RAM write mode**

Note the following when using high-speed RAM write mode.

Note 1: High-speed RAM write mode performs the write operation to the RAM in units of lines. If the written data is less than the number of window addresses in the horizontal line of the window address area, data is not written correctly.

Note 2: When the index register – RAM data write (“202”H) is selected, the BD663474 always performs the first write operation. With this setting, the RAM data read operation is not performed. Set HWM = 0 for the RAM read operation.

Note 3: High-speed RAM write mode is not operable simultaneously with the normal RAM write mode. When switching between modes, set the address before restarting RAM access.

Note 4: Refer to the following table for the relationship between functions and RAM access.

	Normal RAM write (HWM = 0)	High-speed RAM write (HWM = 1)
BGR function	Available	Available
Write mask function	Available	Available
RAM address set	Settable for each word	Settable for each word
RAM read	Available	Not available
RAM write	Settable for each word	Settable for each line
Window address function	Settable for each word (minimum area: 1 word × 1 line)	Settable for each word (minimum area: 8 word × 1 line)
External display interface	Not available	Available
Writing direction (AM)	AM = 1/0	AM = 0

Window Address Function

The BD663474 has a window address function for writing data in an arbitrarily set rectangular area on the GRAM by setting the start and end points of the address. The data of the moving picture area in a still image can be consecutively updated without considering the wrap-around positions of the GRAM address.

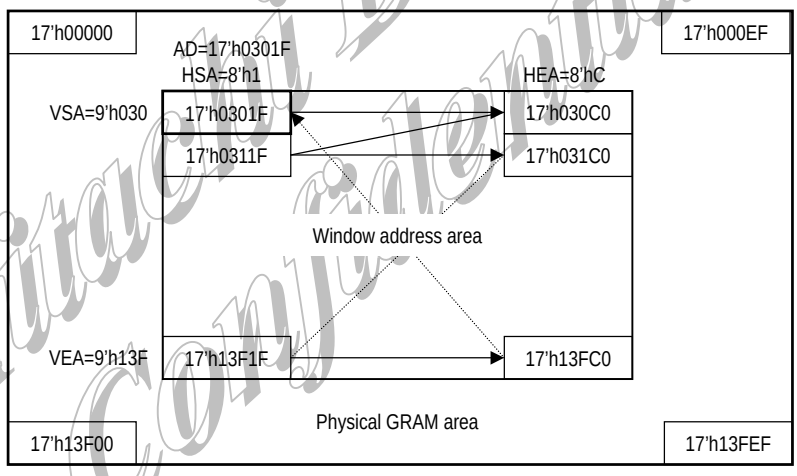
Here are some notes on using the window address function.

Note 1: The start and end points of the window address must be set within the area of the physical address of the GRAM. The following relations must also be observed.

- Horizontal direction : 8'h00 ≤ HSA < HEA ≤ 8'hEF
- Vertical direction : 9'h000 ≤ VSA < VEA ≤ 9'h13F

Note 2: The GRAM start address must be set within the range of the window address area.

- Horizontal address : HSA ≤ AD[7:0] ≤ HEA
- Vertical address : VSA ≤ AD[17:8] ≤ VEA

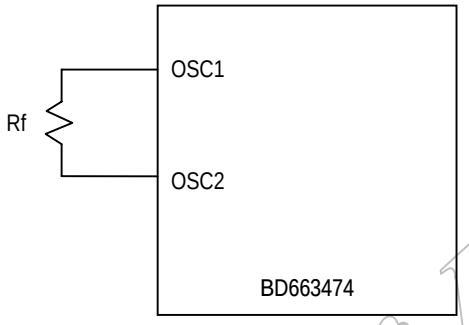


■ Example of window address setting
- ○ HSA=8'h1F HEA=8'hC0
- ○ VSA=9'h030 VEA=9'h13F
- ○ AD=17'h0301F
- ○ AM=1'b0
- ○ I/D=2'b11

Diagram: Example of GRAM address operation in window address area

Oscillator

The BD663474 generates an oscillation with an internal CR oscillator by having an external oscillation resistor placed between the OSC1 and OSC2 pins. The oscillation frequency varies depending on the value of the external resistor and the distance of wiring.
If the resistance value Rf is larger, the oscillation frequency becomes lower. The clock generated by the oscillator circuit is used to generate the control signal for the panel display and DCCLK signal. Refer to “Notes on electrical characteristics” for the relation between the Rf value and the oscillation frequency.



* Place the Rf resistor as close to the OSC1 and OSC2 pins as possible.

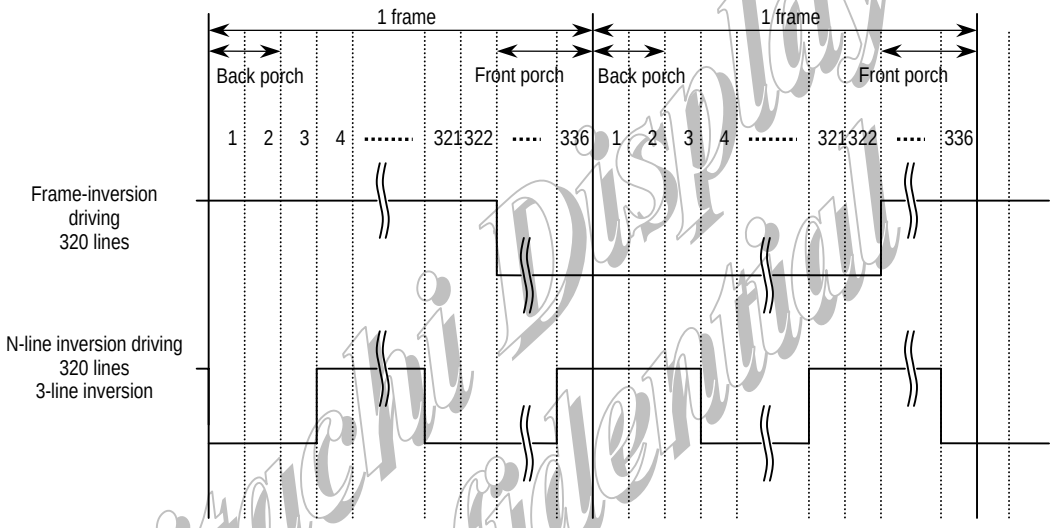
External resistor oscillation mode

n-Line Inversion Liquid Crystal Drive

In addition to the frame-inversion liquid crystal drive, the BD663474 supports the n-line inversion drive, where the polarity of liquid crystal is inverted in units of n lines, where n is a number from one to four. The n-line inversion drive is a function for overcoming problems associated with the quality of the display.

In determining n (NW set value + 1), which represents the number of lines that determines the timing of polarity inversion, check the quality of the display on the liquid crystal panel in use. Note that setting a smaller number of lines raises the frequency of liquid crystal polarity inversion. This results in an increase of charging/discharging current on liquid crystal cells.

[Example of signal timing for n-line inversion liquid crystal drive]



Frame Frequency Adjustment Function

The BD663474 has a frame frequency adjustment function. The frame frequency for driving LCDs can be adjusted by instructions (set with DIVI and RTNI) without changing the oscillation frequency.
To switch between frame frequencies for displaying a moving picture and for displaying a still picture, set a high oscillation frequency in advance. This makes it possible to set a low frame frequency when displaying a still picture to save power, and a high frame frequency when displaying a moving picture to meet the requirement of switching frames at high speed.
In RGB interface and VSYNC interface modes, frame frequency is determined by the VSYNC cycle. Note that the DIVE and RTNE registers are not used to adjust the frame frequency in those modes.

- **Relation between liquid crystal drive duty and frame frequency**

  The relation between the liquid crystal drive duty and frame frequency is calculated from the following equation. The frame frequency can be adjusted by instructions with the 1H period adjustment bits (RTNI) and operation clock division bits (DIVI).

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Number or clock per line} \times \text{Division ratio} \times (\underline{\textit{Line + FP + BP}})} \text{ [Hz]}$$

fosc : CR oscillation frequency
Line : Number of driven lines (NL bit)
Division ratio : DIVI bit
Number of clocks per line : RTNI bit
BP : Number of lines for back porch
FP : Number of lines for front porch

- **Example of calculation: when maximum frame frequency = 60Hz**

  Number of driven lines : NL0 = 320 lines
  1H period : 16 clocks (RTNI[4:0] = 5'h10)
  Division ratio of operating clock : ×1/1 (DIVI [1:0] = 2'b00)
  BP : 8 lines
  FP : 8 lines

  [Formula to calculate frame frequency]

  Fosc = 60Hz × 16 clocks × 1/1 × (320 + 8 + 8) lines = 323 [kHz]

  In this case, the CR oscillation frequency to be set is 323 kHz. Adjust the value of the external resistor connected to the CR oscillator. See “Notes on electrical characteristics” for the relation between the external resistor value and oscillation frequency.

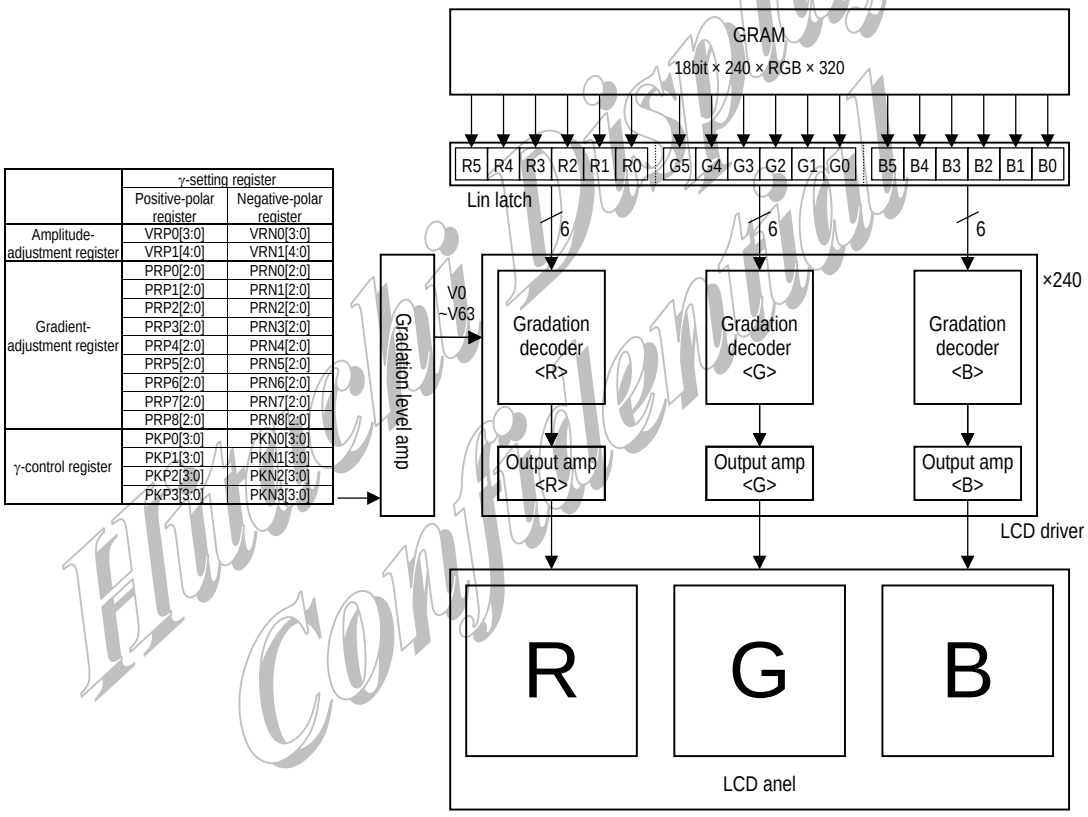
γ-Control Circuit

The BD663474 has a γ-correction function to adjust the display of 262,144 colors. γ-correction is performed with:

- The amplitude-adjustment register
- The gradient-adjustment register
- The fine-adjustment register

Adjusting these registers enables selection of twelve levels of gradation.
Each register has groups for both positive and negative polarities, so they can be set independently to conform to the characteristics of the liquid crystal panel. (Reference values and R, G and B are common.)

	γ-setting register	
	Positive-polar register	Negative-polar register
Amplitude-adjustment register	VRP0[3:0]	VRN0[3:0]
	VRP1[4:0]	VRN1[4:0]
Gradient-adjustment register	PRP0[2:0]	PRN0[2:0]
	PRP1[2:0]	PRN1[2:0]
	PRP2[2:0]	PRN2[2:0]
	PRP3[2:0]	PRN3[2:0]
	PRP4[2:0]	PRN4[2:0]
	PRP5[2:0]	PRN5[2:0]
	PRP6[2:0]	PRN6[2:0]
	PRP7[2:0]	PRN7[2:0]
	PRP8[2:0]	PRN8[2:0]
γ-control register	PKP0[3:0]	PKN0[3:0]
	PKP1[3:0]	PKN1[3:0]
	PKP2[3:0]	PKN2[3:0]
	PKP3[3:0]	PKN3[3:0]



■ Gradation voltage generator circuit

The following diagram shows the configuration of the gradation voltage generator circuit.
The 12 levels of reference voltage (V0, 1, 2, 4, 8, 20, 43, 55, 59, 61, 62 and 63) are determined with each register.
At each level, the voltage is divided through the gradation amplifier to generate 64 levels (V0 – V63).

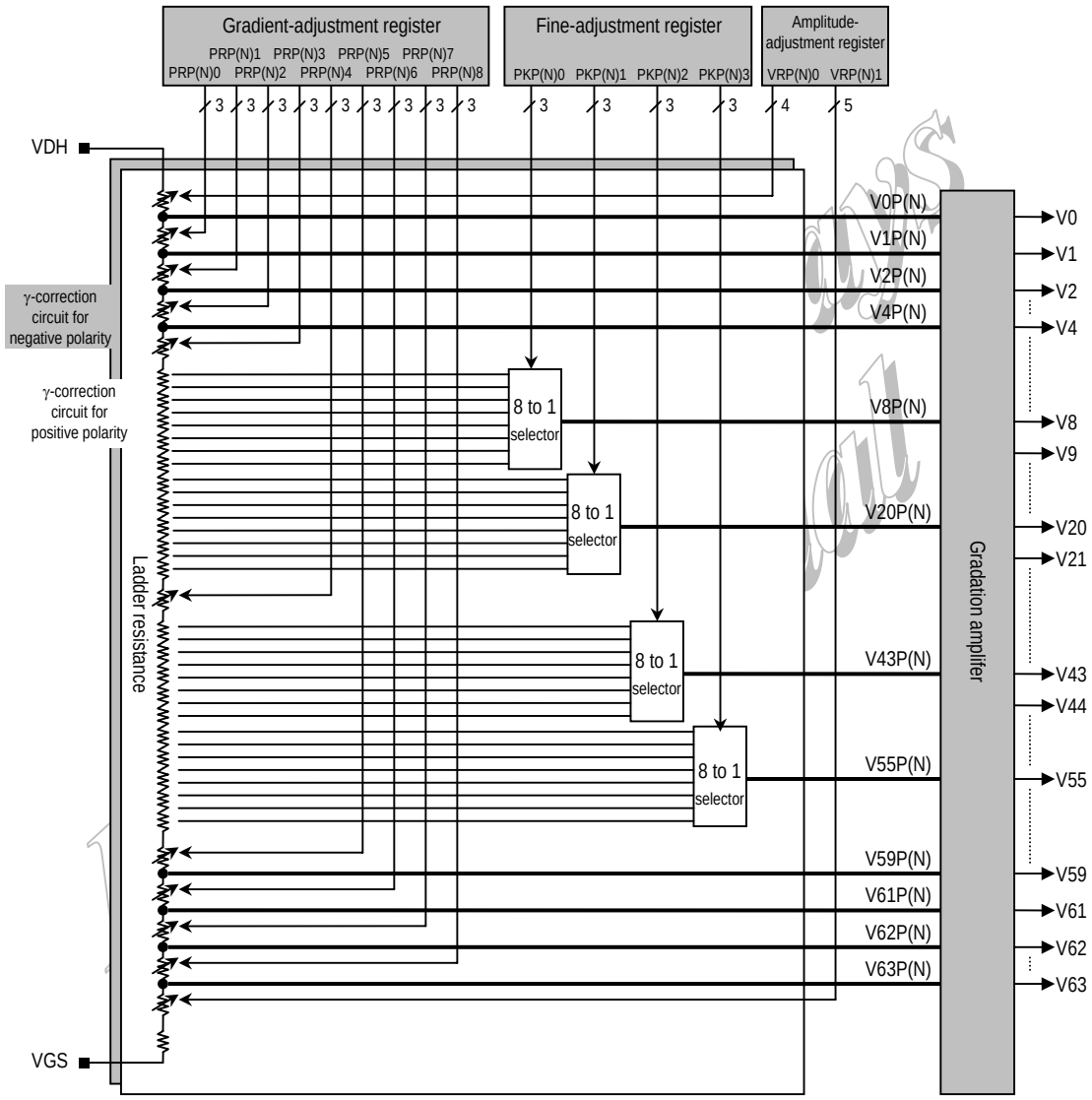


Diagram: Gradation voltage generator circuit

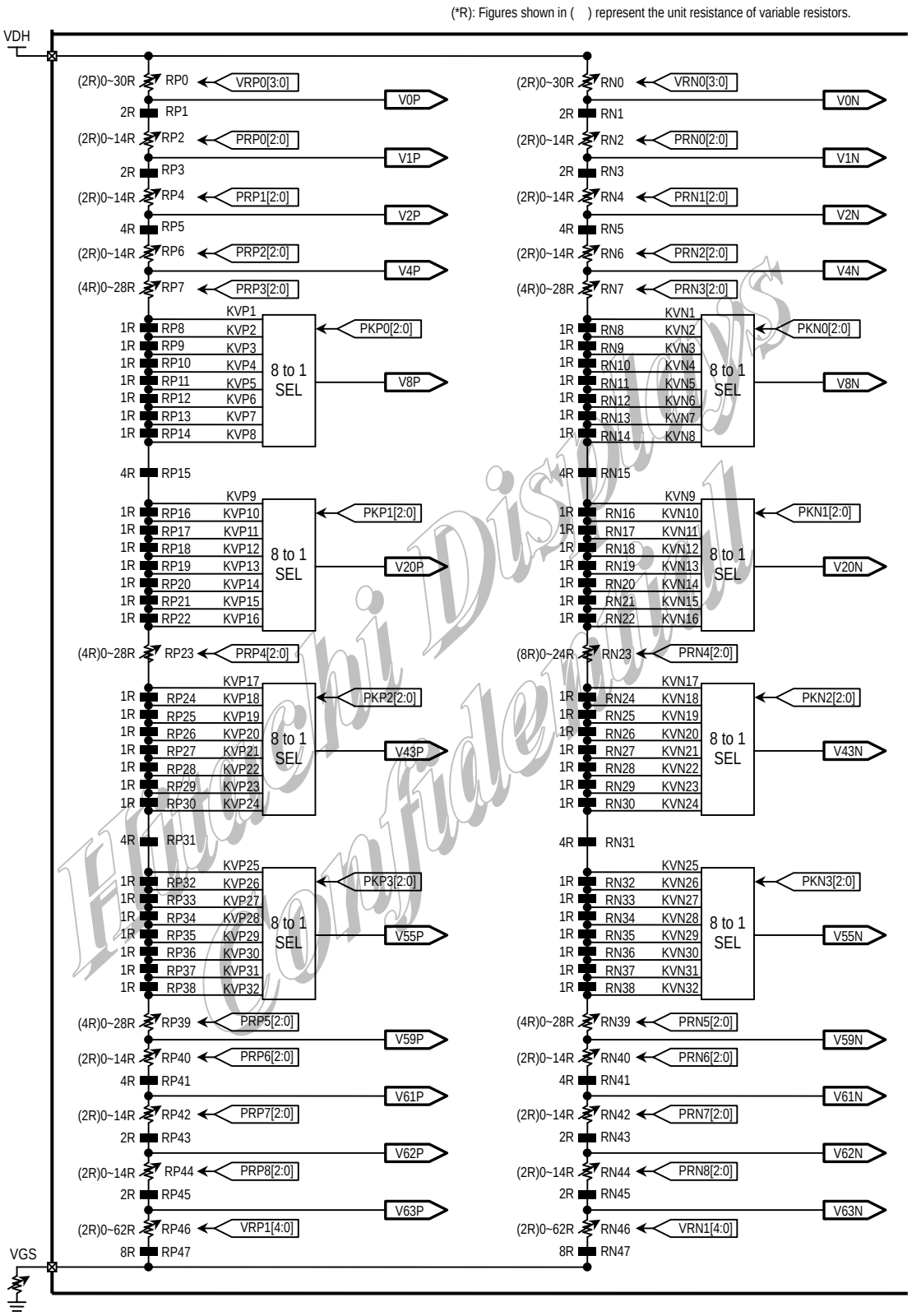
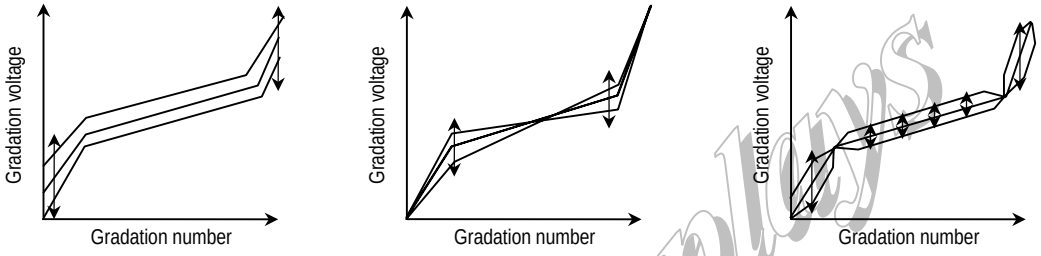


Diagram: γ-control circuit

■ **γ-adjustment registers**

The γ-adjustment register can set the appropriate gradation voltage to conform to the γ -characteristics of the liquid crystal panel in use. The γ-adjustment register includes the following gradient, amplitude and fine adjustment registers, which can perform adjustment in relation to the gradation number and gradation voltage characteristics. Each register group consists of positive and negative polarity registers, which are set independently from one other. The reference values and R, G and B are common. The following diagrams illustrate the operation of each adjustment register. Refer to the γ -control circuit diagram.



Amplitude adjustment **Gradient adjustment** **Fine adjustment**

(1) Amplitude adjustment register (VRP(N))

The amplitude adjustment register is used to adjust the amplitude of the gradation voltage. To adjust the amplitude, the values of the gradation voltage generating variable resistors in the upper and lower parts of the ladder resistor unit are adjusted.

(2) Gradient adjustment register (PRP(N))

The gradient adjustment register is used to adjust the gradient around the middle of the gradation number and the gradation voltage characteristics without changing the dynamic range. To adjust the gradient, the values of the gradation voltage generating variable resistors in the middle of the ladder resistor unit are adjusted.

(3) Fine adjustment register (PKP(N))

The fine adjustment register is used to fine-adjust the gradation voltage level. To perform fine adjustment, each reference voltage level is controlled by the 8-to-1 selector corresponding to the eight reference voltage levels generated by the ladder resistors.

1. Variable resistor

The BD663474 uses two types of variable resistors for the purposes of amplitude adjustment (VRP(N)) and gradient adjustment (PRP(N)). The value of the resistance is determined by the amplitude register and the gradient register as shown in the tables below.

(1) Amplitude adjustment

Register value *VRP(N)0[3:0]	Resistance RP(N)0
0000	0R
0001	2R
0010	4R
0011	6R
0100	8R
0101	10R
0110	12R
0111	14R
1000	16R
1001	18R
1010	20R
1011	22R
1100	24R
1101	26R
1110	28R
1111	30R

Register value *VRP(N)1[4:0]	Resistance RP(N)46	Register value *VRP(N)1[4:0]	Resistance RP(N)46
00000	0R	10000	32R
00001	2R	10001	34R
00010	4R	10010	36R
00011	6R	10011	38R
00100	8R	10100	40R
00101	10R	10101	42R
00110	12R	10110	44R
00111	14R	10111	46R
01000	16R	11000	48R
01001	18R	11001	50R
01010	20R	11010	52R
01011	22R	11011	54R
01100	24R	11100	56R
01101	26R	11101	58R
01110	28R	11110	60R
01111	30R	11111	62R

(2) Gradient adjustment

Register value *PRP(N) 0,1,2,6,7,8[2:0]	Resistance RP(N) 2,4,6,40,42,44
000	0R
001	2R
010	4R
011	6R
100	8R
	10R
110	12R
111	14R

Register value *PRP(N) 3,4,5[2:0]	Resistance RP(N) 7,23,39
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

2. 8-to-1 selector

The 8-to-1 selector selects one voltage level from among the voltage levels generated by the ladder resistor according to the fine adjustment register bits, and outputs it. The following table shows the relation between the value of the fine adjustment register and the selected voltage.

Relation between value of fine adjustment register and selected voltage

Register value *PKP(N) 0,1,2,3[2:0]	Selected voltage			
	V8P(N)	V20P(N)	V43P(N)	V55P(N)
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32

■ **Voltage calculation formula**

Table: Voltage calculation formula

Terminal name	Calculation formula	Fine-adjustment register value	Reference voltage
V0P(N)	VGS + Vpp * [{V1P(N) + 2 + 'PRP(N)0'*2}R/Rall]	-	V0P(N)
V1P(N)	VGS + Vpp * [{V2P(N) + 2 + 'PRP(N)1'*2}R/Rall]	-	V1P(N)
V2P(N)	VGS + Vpp * [{V4P(N) + 4 + 'PRP(N)2'*2}R/Rall]	-	V2P(N)
V4P(N)	VGS + Vpp * [{KVP(N)1 + 'PRP(N)3'*4}R/Rall]	-	V4P(N)
KVP(N)1	VGS + Vpp * [{KVP(N)9 + 4 +7}R/Rall]	*'PKP(N)0'="000"	V8P(N)
KVP(N)2	VGS + Vpp * [{KVP(N)9 + 4 +6}R/Rall]	*'PKP(N) 0'="001"	
KVP(N)3	VGS + Vpp * [{KVP(N)9 + 4 +5}R/Rall]	*'PKP(N) 0'="010"	
KVP(N)4	VGS + Vpp * [{KVP(N)9 + 4 +4}R/Rall]	*'PKP(N) 0'="011"	
KVP(N)5	VGS + Vpp * [{KVP(N)9 + 4 +3}R/Rall]	*'PKP(N) 0'="100"	
KVP(N)6	VGS + Vpp * [{KVP(N)9 + 4 +2}R/Rall]	*'PKP(N) 0'="101"	
KVP(N)7	VGS + Vpp * [{KVP(N)9 + 4 +1}R/Rall]	*'PKP(N) 0'="110"	
KVP(N)8	VGS + Vpp * [{KVP(N)9 + 4}R/Rall]	*'PKP(N) 0'="111"	
KVP(N)9	VGS + Vpp * [{KVP(N)17 + 'PRP(N)4'*4 +7}R/Rall]	*'PKP(N) 1'="000"	V20P(N)
KVP(N)10	VGS + Vpp * [{KVP(N)17 + 'PRP(N)4'*4 +6}R/Rall]	*'PKP(N) 1'="001"	
KVP(N)11	VGS + Vpp * [{KVP(N)17 + 'PRP(N)4'*4 +5}R/Rall]	*'PKP(N) 1'="010"	
KVP(N)12	VGS + Vpp * [{KVP(N)17 + 'PRP(N)4'*4 +4}R/Rall]	*'PKP(N) 1'="011"	
KVP(N)13	VGS + Vpp * [{KVP(N)17 + 'PRP(N)4'*4 +3}R/Rall]	*'PKP(N) 1'="100"	
KVP(N)14	VGS + Vpp * [{KVP(N)17 + 'PRP(N)4'*4 +2}R/Rall]	*'PKP(N) 1'="101"	
KVP(N)15	VGS + Vpp * [{KVP(N)17 + 'PRP(N)4'*4 +1}R/Rall]	*'PKP(N) 1'="110"	
KVP(N)16	VGS + Vpp * [{KVP(N)17 + 'PRP(N)4'*4}R/Rall]	*'PKP(N) 1'="111"	
KVP(N)17	VGS + Vpp * [{KVP(N)25 + 4 + 7}R/Rall]	*'PKP(N) 2'="000"	V43P(N)
KVP(N)18	VGS + Vpp * [{KVP(N)25 + 4 + 6}R/Rall]	*'PKP(N) 2'="001"	
KVP(N)19	VGS + Vpp * [{KVP(N)25 + 4 + 5}R/Rall]	*'PKP(N) 2'="010"	
KVP(N)20	VGS + Vpp * [{KVP(N)25 + 4 + 4}R/Rall]	*'PKP(N) 2'="011"	
KVP(N)21	VGS + Vpp * [{KVP(N)25 + 4 + 3}R/Rall]	*'PKP(N) 2'="100"	
KVP(N)22	VGS + Vpp * [{KVP(N)25 + 4 + 2}R/Rall]	*'PKP(N) 2'="101"	
KVP(N)23	VGS + Vpp * [{KVP(N)25 + 4 + 1}R/Rall]	*'PKP(N) 2'="110"	
KVP(N)24	VGS + Vpp * [{KVP(N)25 + 4}R/Rall]	*'PKP(N) 2'="111"	
KVP(N)25	VGS + Vpp * [{V59P(N) + 'PRP(N)5'*4 + 7}R/Rall]	*'PKP(N) 3'="000"	V55P(N)
KVP(N)26	VGS + Vpp * [{V59P(N) + 'PRP(N)5'*4 + 6}R/Rall]	*'PKP(N) 3'="001"	
KVP(N)27	VGS + Vpp * [{V59P(N) + 'PRP(N)5'*4 + 5}R/Rall]	*'PKP(N) 3'="010"	
KVP(N)28	VGS + Vpp * [{V59P(N) + 'PRP(N)5'*4 + 4}R/Rall]	*'PKP(N) 3'="011"	
KVP(N)29	VGS + Vpp * [{V59P(N) + 'PRP(N)5'*4 + 3}R/Rall]	*'PKP(N) 3'="100"	
KVP(N)30	VGS + Vpp * [{V59P(N) + 'PRP(N)5'*4 + 2}R/Rall]	*'PKP(N) 3'="101"	
KVP(N)31	VGS + Vpp * [{V59P(N) + 'PRP(N)5'*4 + 1}R/Rall]	*'PKP(N) 3'="110"	
KVP(N)32	VGS + Vpp * [{V59P(N) + 'PRP(N)5'*4}R/Rall]	*'PKP(N) 3'="111"	
V59P(N)	VGS + Vpp * [{V61P(N) + 4 + 'PRP(N)6'*2}R/Rall]	-	V59P(N)
V61P(N)	VGS + Vpp * [{V62P(N) + 2 + 'PRP(N)7'*2}R/Rall]	-	V61P(N)
V62P(N)	VGS + Vpp * [{V63P(N) + 2 + 'PRP(N)8'*2}R/Rall]	-	V62P(N)
V63P(N)	VGS + Vpp * [{8 + 'VRP(N)1'*2}R/Rall]	-	V63P(N)

Rall : {SUM(A)*2+SUM(B)*4+'PRP(N)4'*4+2*4+4*4+7*4+8}*R

SUM(A) : {'VRP(N)0'+'VRP(N)1'}+{'PRP(N)0'+'PRP(N)1'+'PRP(N)2'+'PRP(N)6'+'PRP(N)7'+ 'PRP(N)8'}

SUM(B) : 'PRP(N)3'+'PRP(N)5'

Vpp : VDH-VGS

{···} R/Rall : The figures in { } indicate the unit resistances R from the VGS terminal to each terminal (See γ-control circuit diagram). In addition, except for the formula for V63(N), the first terminal names in { } of { } R/Rall indicate the number of unit resistances R used.

e.g. In the case of terminal name V62P(N)

Formula : VGS + Vpp*{V63P(N)+2+'PRP(N)8'*2}R/Rall

V63P(N) in the formula equal to {8+'VRP(N)1'*2} shown in the formula for V63P(N).

Register value : Decimal number of set value.

The table below shows the formulae for calculating V0 to V63.

The 64 levels from V0 to V63 are generated based on the reference voltages of 12 levels (V0, 1, 2, 4, 8, 20, 43, 55, 59, 61, 62 and 63).

Table: Voltage calculation formulae

Gradation voltage	Calculation formula
V0	V0P, V0N
V1	V1P, V1N
V2	V2P, V2N
V3	V4+(V2-V4)*(1/2)
V4	V4P,V4N
V5	V8+(V4-V8)*(3/4)
V6	V8+(V4-V8)*(2/4)
V7	V8+(V4-V8)*(1/4)
V8	V8P, V8N
V9	V20+(V8-V20)*(11/12)
V10	V20+(V8-V20)*(10/12)
V11	V20+(V8-V20)*(9/12)
V12	V20+(V8-V20)*(8/12)
V13	V20+(V8-V20)*(7/12)
V14	V20+(V8-V20)*(6/12)
V15	V20+(V8-V20)*(5/12)
V16	V20+(V8-V20)*(4/12)
V17	V20+(V8-V20)*(3/12)
V18	V20+(V8-V20)*(2/12)
V19	V20+(V8-V20)*(1/12)
V20	V20P, V20N
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)

Gradation voltage	Calculation formula
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	V43P, V43N
V44	V55+(V43-V55)*(11/12)
V45	V55+(V43-V55)*(10/12)
V46	V55+(V43-V55)*(9/12)
V47	V55+(V43-V55)*(8/12)
V48	V55+(V43-V55)*(7/12)
V49	V55+(V43-V55)*(6/12)
V50	V55+(V43-V55)*(5/12)
V51	V55+(V43-V55)*(4/12)
V52	V55+(V43-V55)*(3/12)
V53	V55+(V43-V55)*(2/12)
V54	V55+(V43-V55)*(1/12)
V55	V55P, V55N
V56	V59+(V55-V59)*(3/4)
V57	V59+(V55-V59)*(2/4)
V58	V59+(V55-V59)*(1/4)
V59	V59P, V59N
V60	V61+(V59-V61)*(1/2)
V61	V61P, V61N
V62	V62P, V62N
V63	V63P, V61N

Note: Keep the following relations:

V20 > DDVDH/2 – 0.5V

V43 < DDVDH/2 + 0.5V

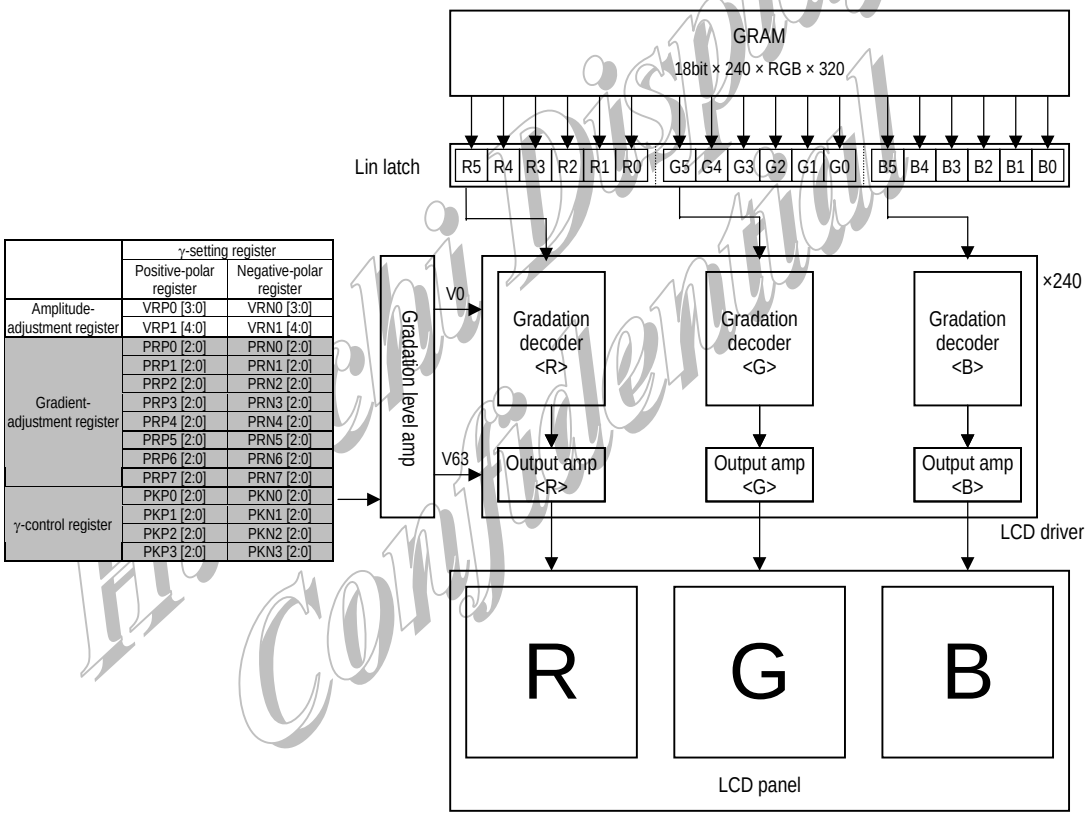
V63 > 0.5V

(When DDVDH ≥ 4.8V)

8-Color Display Mode

The BD663474 has a function for displaying in eight colors, where the available gradations are only V0 and V63, and the voltage supplies for other gradations (V1 to V62) are cut.
In combination with off-scan setting (PTG, PTS and ISC), a standby display in partial display mode can be driven with less power consumption.

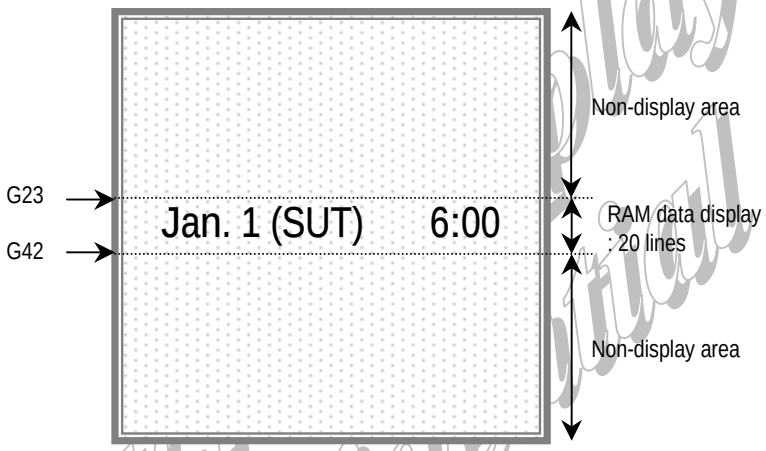
In 8-color display mode, the gradient adjustment register (PRP/PRN) and fine adjustment register (PKP/PKN) are disabled. Since the voltage supplies for V1 to V62 are stopped in 8-color display mode, the display data is automatically converted to select either V0 or V63 by writing the MSB to the remaining five bits of each RGB dot. The BD663474 allows switching between 8-color display mode and normal mode without rewriting GRAM data by just setting the CL register.



Partial Display Function

The BD663474 allows partial display by setting BASEE bit = 0 and PTDE0/1 bit = 1. Areas other than the display area become non-display areas so that the BD663474 drives the LCD with reduced power consumption. RAM data in an arbitrary area can be displayed at an arbitrary position, by setting the RAM area (PTSA0/1, PTEA0/1) and the display start position (PTDP0/1). Two partial display areas can be set.
In combination with the 8-color display mode and off-scan setting (PTG, PTS, ISC), the BD663474 can drive the display with less power consumption. Adjust while checking the quality of the display.

- **Setting example for partial display drive**



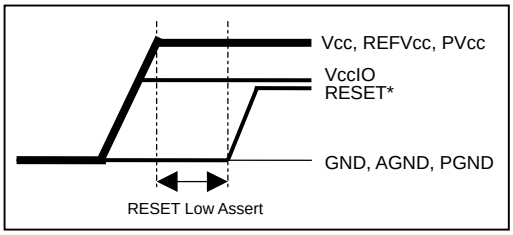
Number of driven lines	: NL = 6'h07 (64 lines)
Base image display enable	: BASEE = 0
Partial display enable	: PTDE0 = 1
Partial display first screen RAM area	: (PTSA0, PTEA0)=(8'h000, 8'h013)
Partial display first screen start position	: PTDP0 = 8'h016

See “Display RAM address and position on panel” for the display area and the setting for the RAM area.

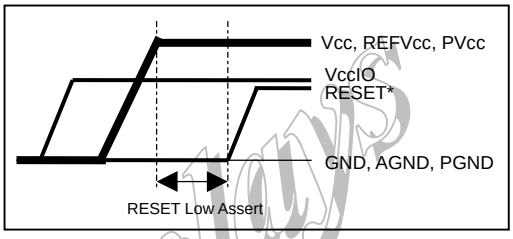
Instruction Setup Flow

■ **Power supply ON sequence**

Turn on the power of VccIO, Vcc, REFVcc and PVcc in that order, or all simultaneously. Always set RESET* to GND level when turning on the power.

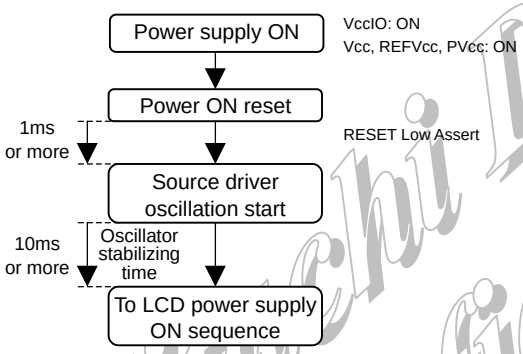


Power supply ON sequence (1)



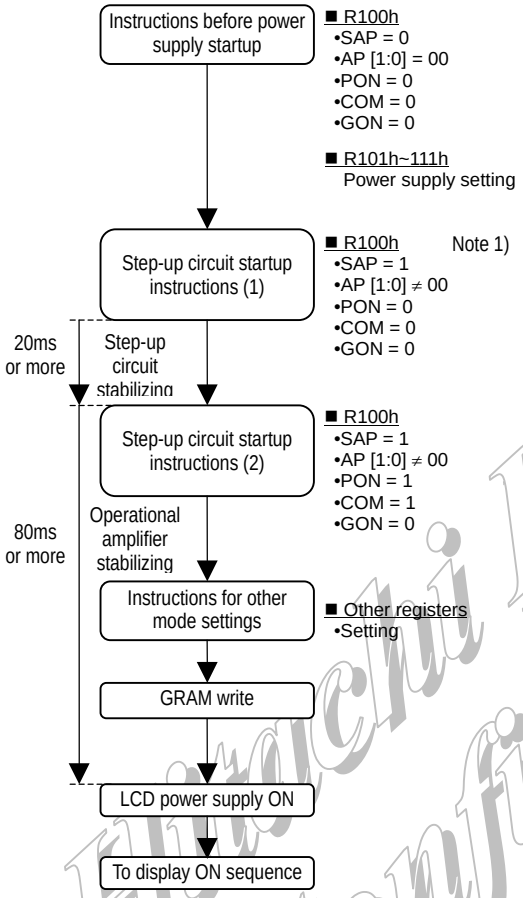
Power supply ON sequence (2)

[Power supply ON sequence]

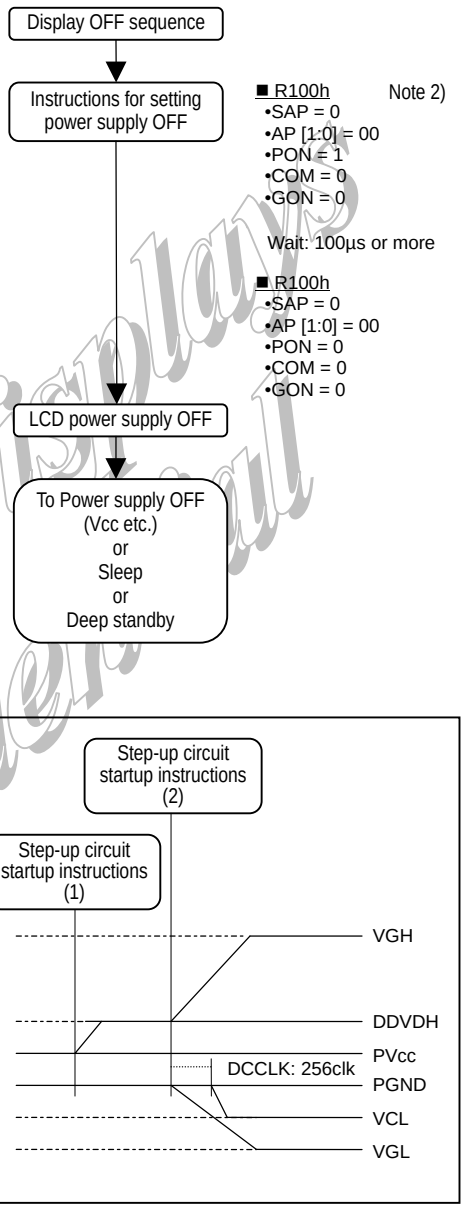


■ **LCD power supply sequence**

[LCD Power supply ON sequence]



[LCD Power supply OFF sequence]



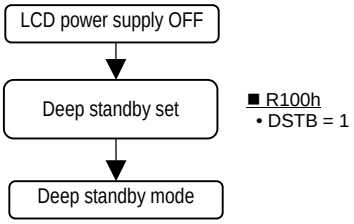
Note 1: Complete setting AP [1:0] before setting PON = 1. No change to AP [1:0] is accepted while PON = 1, except setting AP[1:0] = 00 during the LCD power supply off sequence. See Note 2.

Note 2: Set PON = 0 after transferring AP [1:0] = 00 to the BD663474 when the LCD power supply is turned off.

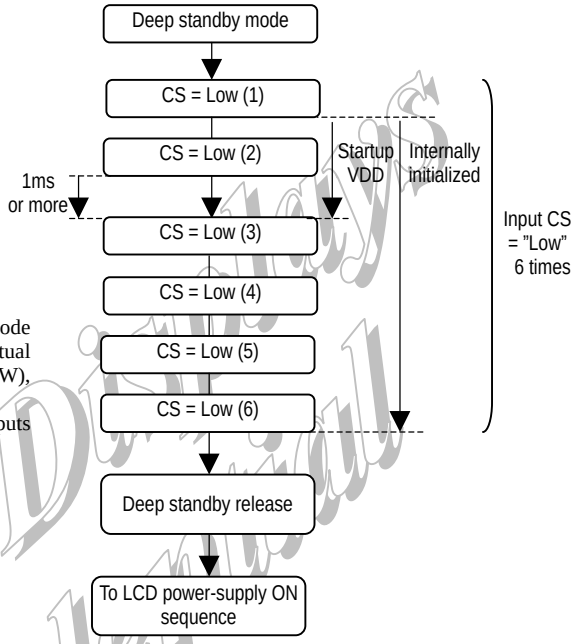
■ Deep standby and Sleep modes

(1) Deep standby

[Sequence to Deep standby mode]



[Deep standby release] Note1) Note2)

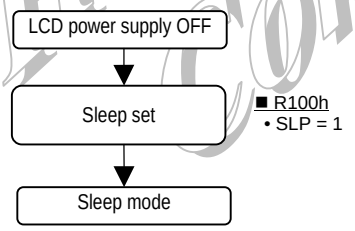


Note 1: Refer to AC characteristics of each interface mode in “Electrical characteristics” for details on actual time of low width (PWLW), high width (PWHW), and cycle (tCYCW).

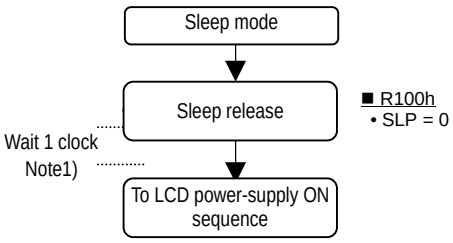
Note 2: Leave at least 1ms between second and third inputs of CS = ”Low” after release from deep standby.

(2) Sleep

[Sequence to sleep mode]

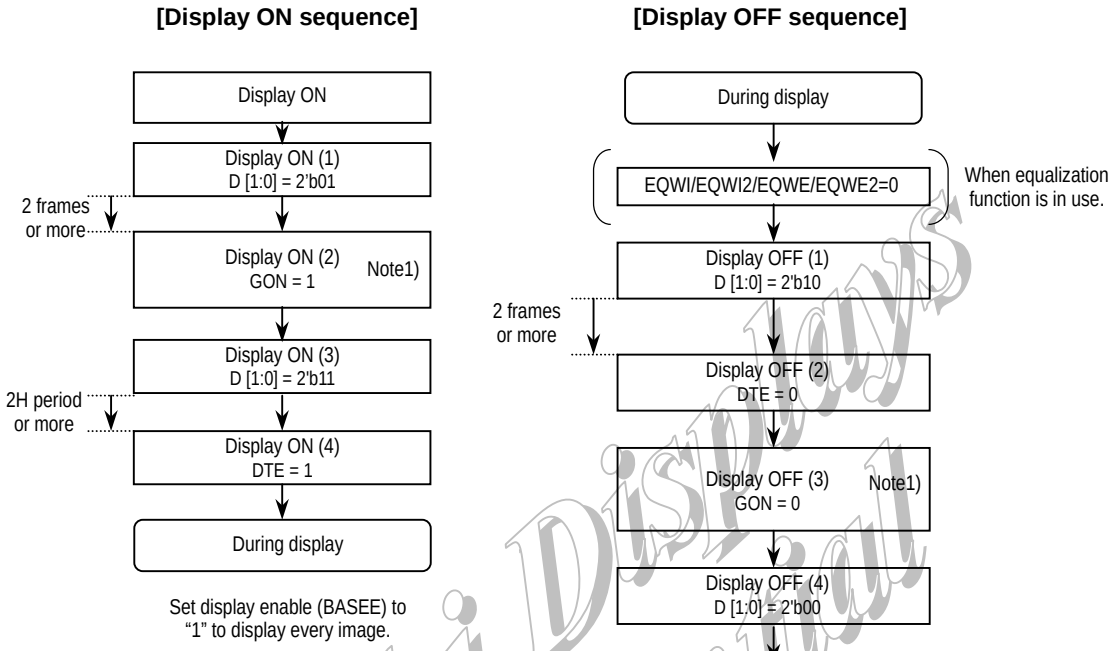


[Sleep release]



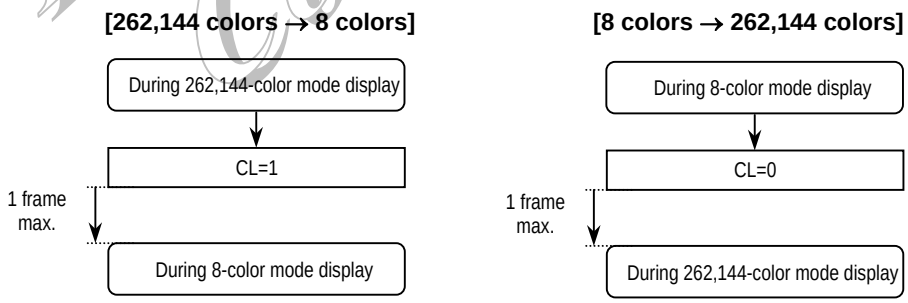
Note 1: Internal oscillation clock OSC1

■ Display ON/OFF sequences

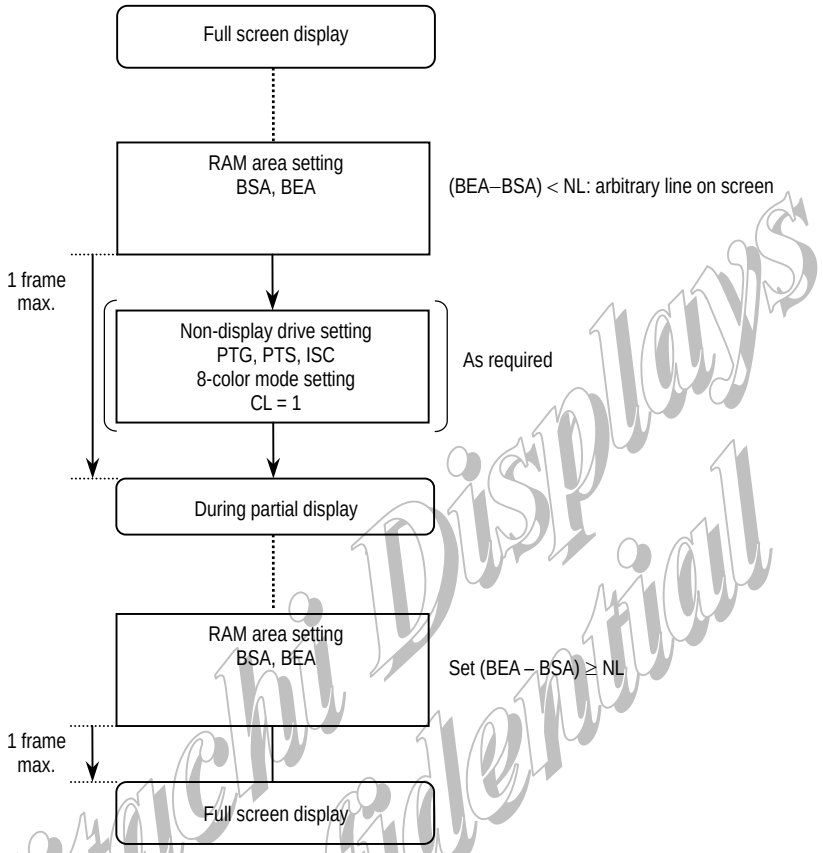


Note 1: Do not set GON = 1 when D = 2'b00.

■ 8-color display mode

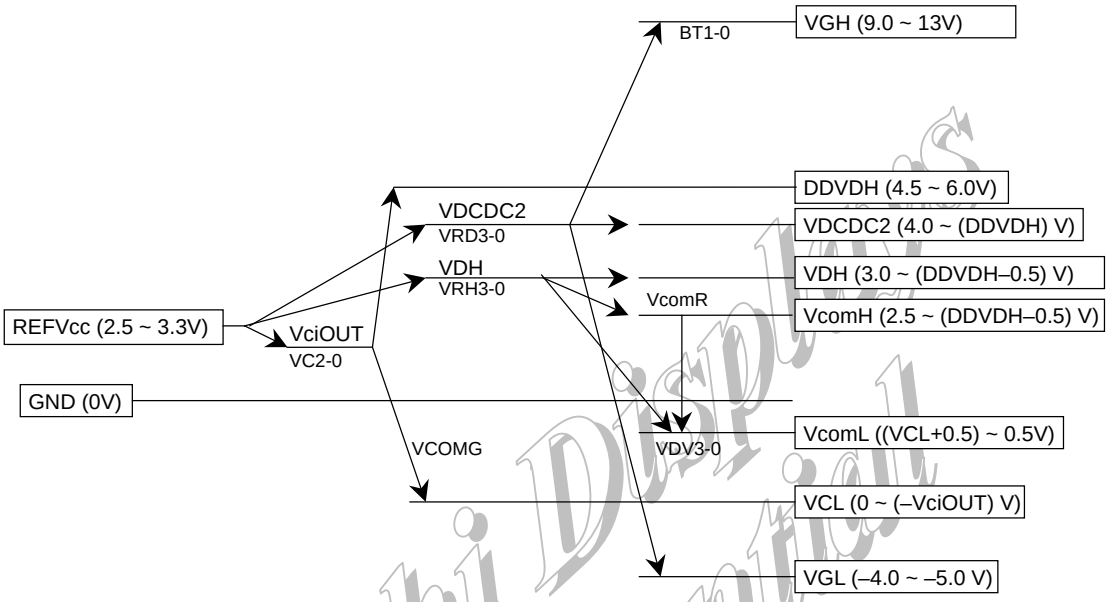


■ **Partial display mode**



Pattern Diagram for Voltage Setting

■ **Pattern diagram for voltage setting**



Notes: The output voltage levels of DDVDH, VGH, VGL, and VCL become lower than the set voltage (ideal voltage level), depending on current consumption. The relation to the actual voltage is shown by:

(DDVDH-VDH) > 0.5V

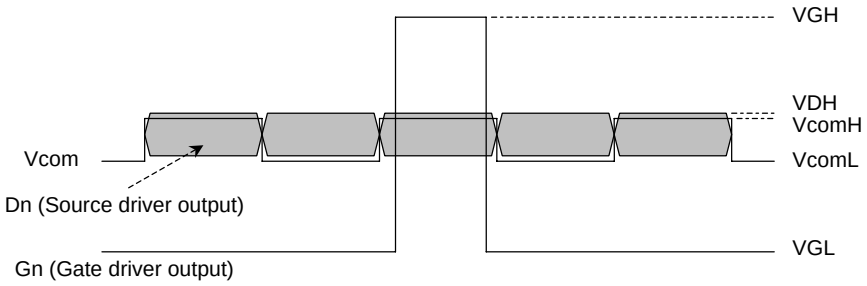
(DDVDH-VcomH) > 0.5V

(VcomL-VCL) > 0.5V

Before using with a large current consumption when Vcom alternation is fast (line inversion drive, etc.), check the actual voltage.

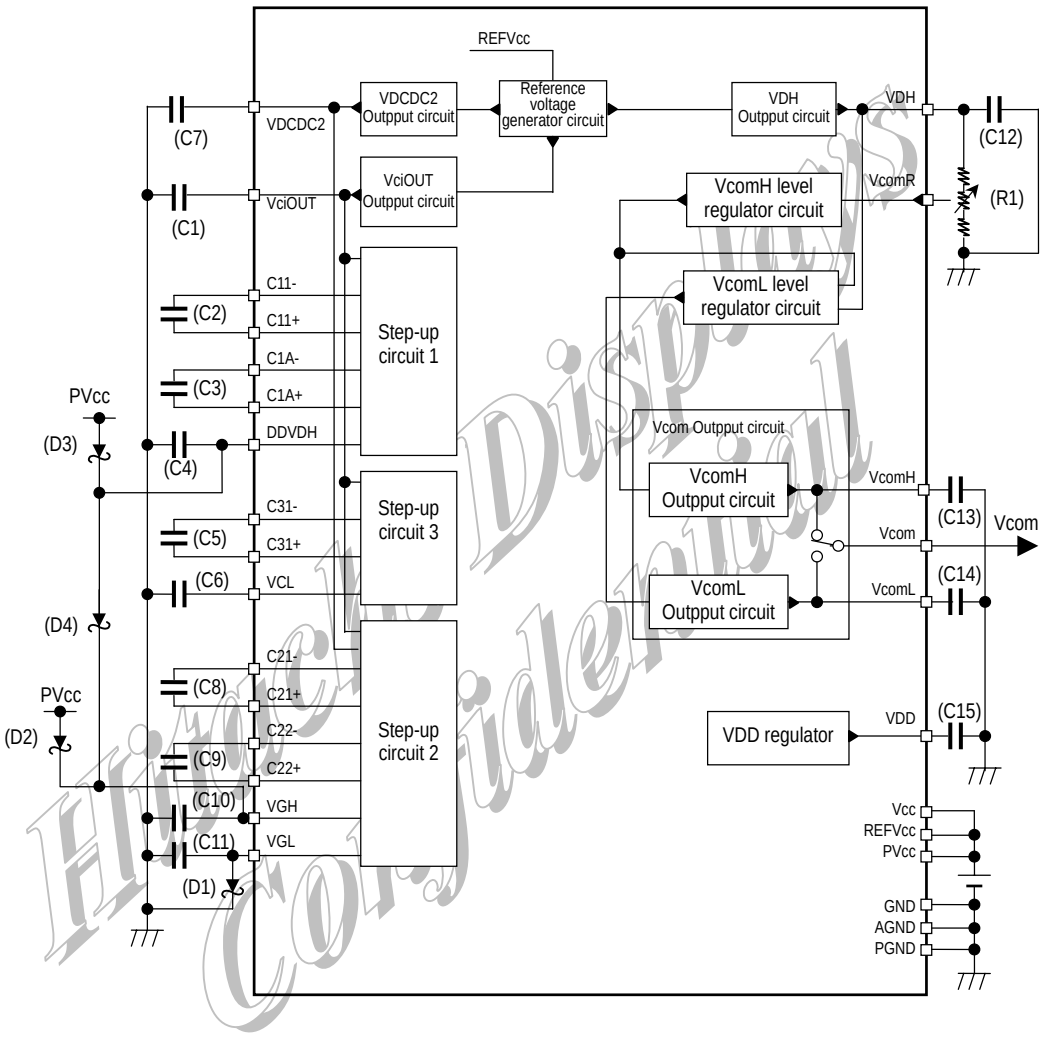
- TFT-display applied voltage

  The diagram below illustrates the waveform of the applied voltage.



External Element Specifications

The following figure shows the configuration of the power supply circuit. The specifications of the external components are shown on the next page.



External component specifications

Capacitor	Recommended capacitance /applied voltage	Recommended voltage	Note
(C1) VciOUT	1μF / VciOUT	6V or more	Required according to instruction “VC”.
(C2) C11±	1μF / VciOUT	6V or more	
(C3) C1A±	1μF / VciOUT	6V or more	Required according to instruction “CA”
(C4) DDVDH	1μF / DDVDH	10V or more	
(C5) C31±	1μF / VciOUT	6V or more	Required according to instruction “VCOMG”
(C6) VCL	1μF / VCL	6V or more	Required according to instruction “VCOMG”
(C7) VDCDC2	1μF / VDCDC2	10V or more	Required according to instruction “APR”
(C8) C21±	1μF / VDCDC2	10V or more	
(C9) C22±	1μF / VDCDC2	10V or more	Required according to instruction “BT”
(C10) VGH	1μF / VGH	25V or more	
(C11) VGL	1μF / VGL	10V or more	
(C12) VDH	1μF / VDH	10V or more	
(C13) VcomH	1μF / VcomH	10V or more	
(C14) VcomL	1μF / VcomL	6V or more	Required according to instruction “VCOMG”
(C15) VDD	1μF / VDD	3V or more	

* Use B-characteristic capacitors.

Other components	Specifications	Note
(D1) ~ (D4)	VF < 0.4V / 20mA@25°C	Connect a Schottky barrier diode
(R1) VcomR	>200kΩ	

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Note
Power supply voltage	Logic circuit	VccIO	–0.3 ~ +4.0	V	(1)
	LCD drive circuit	Vcc – GND REFVcc – GND PVcc – GND	–0.3 ~ +4.0	V	(1)
		DDVDH – GND	–0.3 ~ +6.5	V	(1)
		GND – VCL	–0.3 ~ +3.8	V	(1)
		VciOUT – VCL	–0.3 ~ +6.5	V	
		DDVDH – VCL	–0.3 ~ +10.0	V	
		VGH – GND	–0.3 ~ +15.0	V	(1)
		GND – VGL	–0.3 ~ +6.5	V	(1)
Input voltage		VT1	–0.3 ~ VccIO+0.3	V	(1)
Operative temperature		topr	–40 ~ +85	°C	
Storage temperature		Tstg	–55 ~ +110	°C	

Note(1): Using the LSI beyond the absolute maximum ratings may cause permanent failure of the LSI.
In normal operation, it is preferable to use the LSI under the electrical characteristic conditions. Exceeding these conditions can cause the LSI to malfunction and affect its reliability.

Note(2): The electrical potential of the substrate for this LSI is GND. The electrical connection on the other side of the chip must be kept insulated or at the GND level. If an electrical potential other than GND is applied on the other side of the chip, the LSI's electrical characteristics and operating reliability can not be guaranteed.

Electrical Characteristics

- DC characteristics

Item	Symbol	Measurement conditions	min.	typ.	max.	Unit	Note
Power supply voltage	VccIO	※1	1.65	—	3.3	V	
	Vcc REFVcc PVcc	※1	2.5	—	3.3	V	
Input voltage(1) (except EDI)	VIH1	VccIO=1.65~3.3V	0.80× VccIO	—	VccIO	V	(2)(3)
	VIL1	VccIO=1.65~3.3V	0	—	0.20× VccIO	V	(2)(3)
Input voltage(2) (EDI)	VIH2	Vcc=2.5~3.3V	0.80× Vcc	—	Vcc	V	(2)(3)
	VIL2	Vcc=2.5~3.3V	0	—	0.20× Vcc	V	(2)(3)
Output voltage(1) (except ECS, ESK, and EDO)	VOH1	VccIO=1.65~3.3V IOH=-0.1mA	0.80 × VccIO	—	—	V	(2)(3)
	VOL1	VccIO=1.65~3.3V IOL=0.1mA	—	—	0.20× VccIO	V	(2)(3)
Output voltage(2) (ECS, ESK and EDO)	VOH2	Vcc=2.5~3.3V IOH=-0.1mA	0.80× Vcc	—	—	V	(2)(3)
	VOL2	Vcc=2.5~3.3V IOL=0.1mA	—	—	0.20× Vcc	V	(2)(3)
Gate driver On registance	RONH	VGH-VGL=18V Iload=±0.1mA ※2	—	—	10	KΩ	
	RONL		—	—	10	KΩ	
Input leakage current	IIL	Vin=0V～VccIO または Vcc	-1	—	1	μA	(4)
Current consumption (VccIO-GND) +(Vcc-GND) +(REFVcc-GND) +(PVcc-GND)	Iop1	※3	—	2	2.6	mA	(5)(6)
	Iop2	※4	—	0.35	—	mA	(5)(6)
	Idstb	※5	—	0.15	1	μA	(5)
Output voltage deviation	ΔVo		—	5	—	mV	(7)
Average output voltage deviation	ΔVΔ		—	—	35	mV	(8)

※1 It is range of motion.

※2 The registance values between the G*pin and Vpins(VGH or VGL) when the load current flows one of G1 to G320 pins.
The test condition is the following.
G1 to 320 pins are left open that are not measured.
VGH=13V,VGL=-5V,Iload=±0.1mA

※3 VccIO=Vcc=REFVcc=PVcc=3.0V,Ta=25℃,fOSC=385kHz
262k colors,320line drive,B/C=0, RAM: ALL18'h00000,γ settings: default

※4 VccIO=Vcc=REFVcc=PVcc=3.0V,Ta=25℃,fOSC=385kHz
8 colors,320line drive,RAM: ALL18'h00000,γ settings: default

※5 VccIO=Vcc=REFVcc=PVcc=3.0V,Ta=25℃,In deep-standby

■ **AC characteristics (VccIO=1.65~3.3V, Vcc=PVcc=REFVcc2.5~3.3V,GND=0V)** (note 1)

- Clock characteristics

Item	Symbol	Unit	Measurement conditions	min.	typ.	max.	note
CR oscillation clock	fOSC	kHz	Rf=150kΩ	252	315	378	(9)

- 80-series bus interface (Write sequence)

Item		Symbol	Unit	Measurement conditions	min.	typ.	max.
Bus cycle time	1trans, HWM=0	tCYCW	ns	Fig. 1	150	—	—
	2/3trans				75	—	—
	HWM=1				75	—	—
Write low level pulse width		PWLW	ns	Fig. 1	40	—	—
Write high level pulse width		PWHW	ns	Fig. 1	25	—	—
Write pulse rising edge, falling edge times		tWRr/tWRf	ns	Fig. 1	—	—	25
Address setup time		tASW	ns	Fig. 1	0	—	—
Address hold time		tAHW	ns	Fig. 1	6	—	—
Write data setup time		tDSW	ns	Fig. 1	20	—	—
Write data hold time		tH	ns	Fig. 1	5	—	—

- 80-series bus interface (Read sequence)

Item	Symbol	Unit	Measurement conditions	min.	typ.	max.
Bus cycle time	tCYCR	ns	Fig. 1	500	—	—
Read low level pulse width	PWLR	ns	Fig. 1	250	—	—
Read high level pulse width	PWHR	ns	Fig. 1	200	—	—
Read pulse rising edge, falling edge time	tRDr/tRDf	ns	Fig. 1	—	—	25
Address setup time	tASR	ns	Fig. 1		—	—
Address hold time	tAHR	ns	Fig. 1		—	—
Read data delay time	tDDR	ns	Fig. 1	—	—	200
Read data hold time	tDHR	ns	Fig. 1	5	—	—

- Reset timing characteristics

Item	Symbol	Unit	Measurement conditions	min.	typ.	max.
Reset low level pulse width	tRES	ms	Fig. 4	1	—	—
Reset rising edge time	trRES	μs	Fig. 4	—	—	10

- Serial peripheral interface (Write sequence)

Item	Symbol	Unit	Measurement conditions	min.	typ.	max.
Serial clock cycle time	tSCYCW	ns	Fig. 2	100	—	20000
Serial clock low level pulse width	tSCH	ns	Fig. 2	40	—	—
Serial clock high level pulse width	tSCL	ns	Fig. 2	40	—	—
Serial clock rising edge, falling edge time	tSCr/tSCf	ns	Fig. 2	—	—	20
Chip select setup time	tCSU	ns	Fig. 2	20	—	—
Chip select hold time	tCH	ns	Fig. 2	60	—	—
Serial data input setup time	tSISU	ns	Fig. 2	30	—	—
Serial data input hold time	tSIH	ns	Fig. 2	30	—	—

- Serial Peripheral Interface(Read Sequence)

Item	Symbol	Unit	Measurement conditions	Min.	typ.	max.
Serial clock cycle time	tSCYCR	ns	Fig. 2	350	—	20000
Serial clock low level pulse width	tSCH	ns	Fig. 2	150	—	—
Serial clock high level pulse width	tSCL	ns	Fig. 2	150	—	—
Serial clock rising edge, falling edge time	tSCr/tSCf	ns	Fig. 2	—	—	20
Chip select hold time	tCH	ns	Fig. 2	60	—	—
Serial data output setup time	tSOD	ns	Fig. 2	—	—	130
Serial data output hold time	tSOH	ns	Fig. 2	5	—	—

- RGB interface

Item		Symbol	Unit	Measurement conditions	Min.	typ.	Max.
DOTCLK cycle time	1trans	tCYCD	ns	Fig. 3	100	—	—
	3trans				60	—	—
DOTCLK low level pulse width		PWDL	ns	Fig. 3	25	—	—
DOTCLK high level pulse width		PWDH	ns	Fig. 3	25	—	—
VSYNC setup time		tVSYNCS	clock	Fig. 3	0	—	
HSYNC setup time		tHSYNCS	clock	Fig. 3	0	—	
ENABLE setup time		tENS	ns	Fig. 3	10	—	—
ENABLE hold time		tENH	ns	Fig. 3	20	—	—
RGB data setup time		tPDS	ns	Fig. 3	10	—	—
RGB data hold time		tPDH	ns	Fig. 3	20	—	—
DOTCLK/VSYNC/HSYNC rising edge, falling edge times		trgbr / trgbf	ns	Fig. 3	—	—	20

- LC driver output characteristics

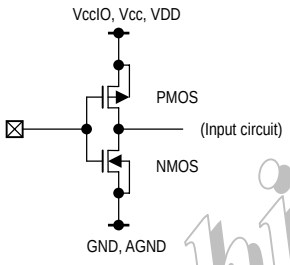
Item	Symbol	Unit	Measurement conditions	min.	typ.	max.
Driver output delay time	tdd	μs	Vcc=2.8V,Ta=25°C,fOSC=500kHz DDVDH=5.5V,VDH=5.0V Load resistance 9kΩ, Load capacity 72pF Ideal value ±35mV arrival time	—	30	—

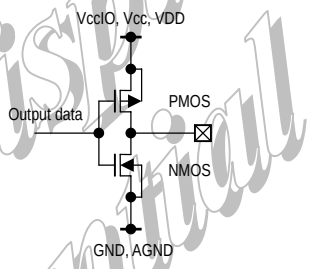
■ **Notes on electrical characteristics**

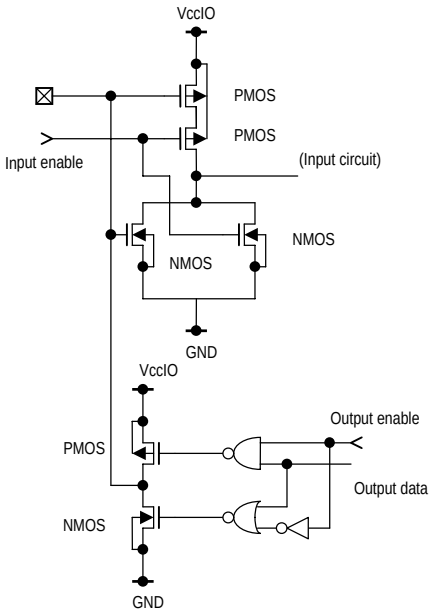
Note 1) DC/AC characteristics of shipped chips and shipped wafers are guaranteed at 85°C.

Note 2) The following Figure illustrates the configurations of input pin, input / output pin, and output pin.

Voltage amplitude	Pins
VccIO-GND	RESET*, IM3-0, CS*, RS, WR*/SCL, RD*, DB17-0, SDI, SDO, VSYNC, HSYNC, DOTCLK, ENABLE, BST, TEST1, VDDTEST, CPTEST, VciTEST, OSC3, TS8-0, TOUT1-3, VCCIODMY, GNDDMY
Vcc-GND	ECS, ESK, EDI, EDO
VDD-GND	OSC1, OSC2, TSC







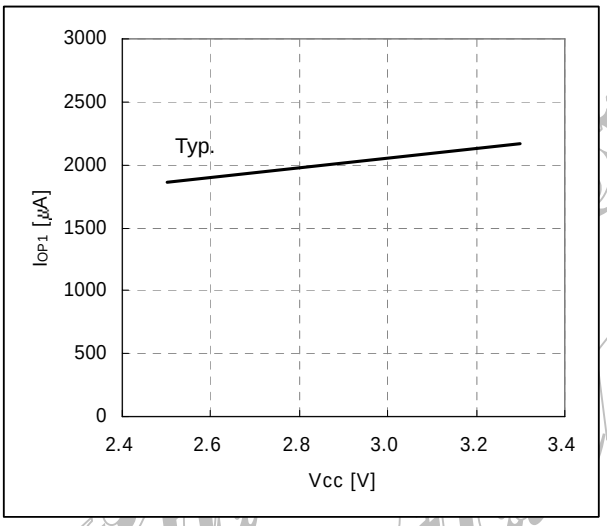
Note 3) TEST1, TSC ,VDDTEST, CPTEST and VciTEST pins must be fixed to GND. IM3-0 pins must be fixed to VccIO or GND.

Note 4) Excluding the current flowing through the output drive MOS.

Note 5) Excluding the current flowing through the input / output units. Make sure that the input level is fixed because transient current in the input circuit will increase when the CMOS level is middle level. The current consumption is unaffected by whether the CS* pin is high or low while no access through the interface pin is being executed.

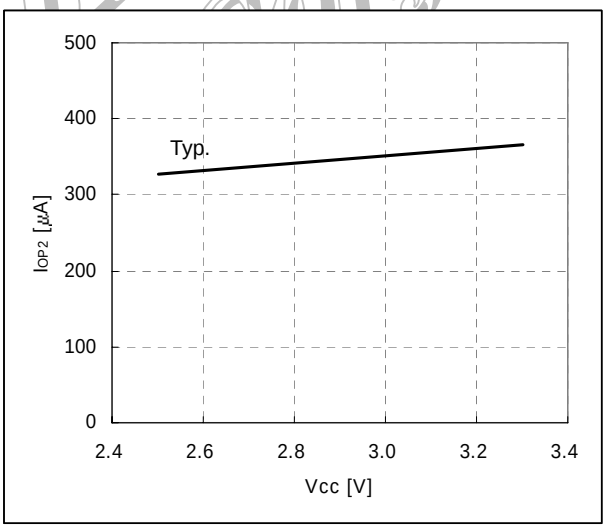
Note 6) The relationship between the operational condition and the current consumption is as follows (for reference).

Opeleating current during 262k colors display（I_{lop1}）



Vcc=VccIO=REFVcc=PVcc
fOSC=385kHz（320 line drive）
fFLM=70Hz, Ta=25℃
B/C=0, REV=0, CL=0, HYP=HIZ=2'h0
AP=2'h2, BT=2'h0, VRD=4'hA, CA=1
APR=2'h1, VRH=4'h7, VDV=4'h9
CHU=CLU=2'h1
RAMdata:ALL 18'h00000
γ setting:default
No panel load

Opeleating current during 8 colors display（I_{op2}）



Vcc=VccIO=REFVcc=PVcc
fOSC=385kHz（(320 line drive）
fFLM=70Hz, Ta=25℃
B/C=0, REV=0, CL=1, HYP=HIZ=2'h0
AP=2'h2, BT=2'h0, VRD=4'hA, CA=0
APR=2'h1, VRH=4'h7, VDV=4'h9
CHU=CLU=2'h0
RAM data： ALL 18'h00000
γ setting:default
No panel load

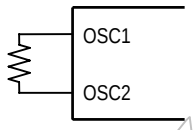
Note 7) The output voltage deviation is the difference in the voltages of adjacent outputs for the same display data. This value is shown as a reference.

Note 8) The average output voltage deviation is the difference in the average output voltage among chips. The average output voltage is measured for each chip with the same display data.

Note 9) This applies to the operation of the internal oscillator with an external oscillation resistor Rf.

[Referential data]

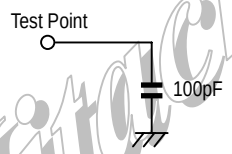
Oscillation resistance [kΩ]	Oscillation frequency [kHz]
75	848
110	616
120	563
130	529
150	468
180	396
220	336
240	305
270	266



Oscillation frequency varies depending on the capacities of OSC1 and OSC2 pins. Check the actual oscillation frequency before use.

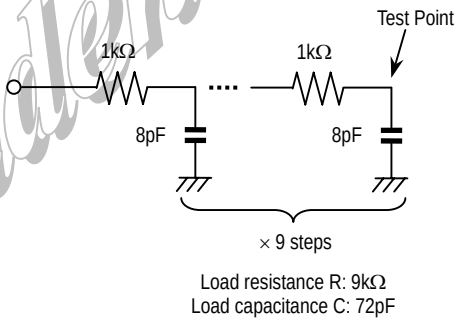
- AC characteristic measurement load equivalent circuit

[Data bus : DB17–0]

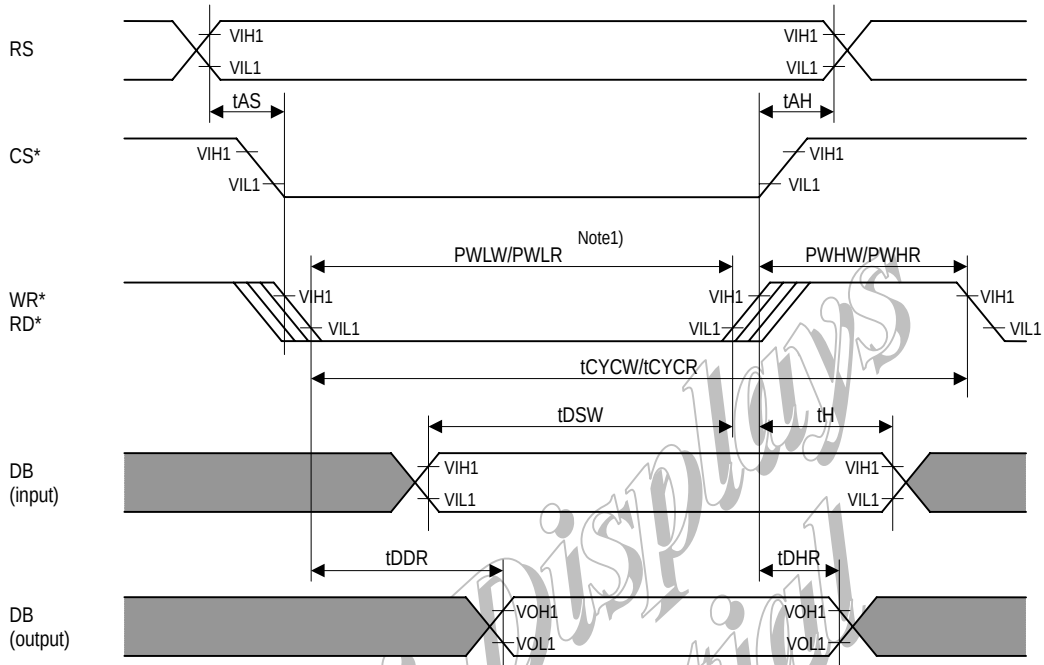


- LC driver output characteristic measurement load equivalent circuit

[LCD output : S1 – S720]



- 80-series bus interface operation



Note 1: PWLW and PWLR in the normal write/read sequences are determined by the overlap period when CS* = Low and WR* or RD* = Low.

Figure 1: 80-series bus interface timing

- Serial peripheral interface (SPI) operation

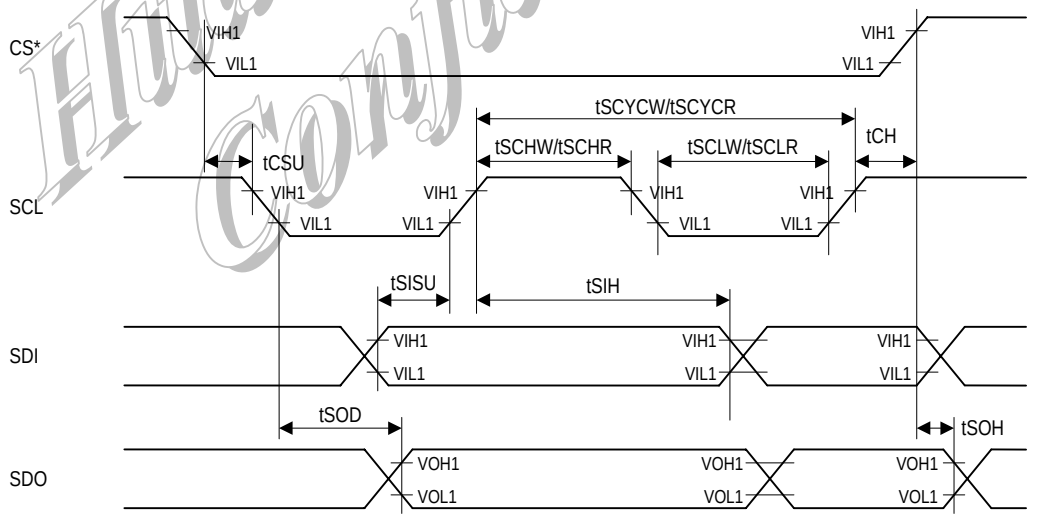


Figure 2: SPI timing

- RGB interface operation

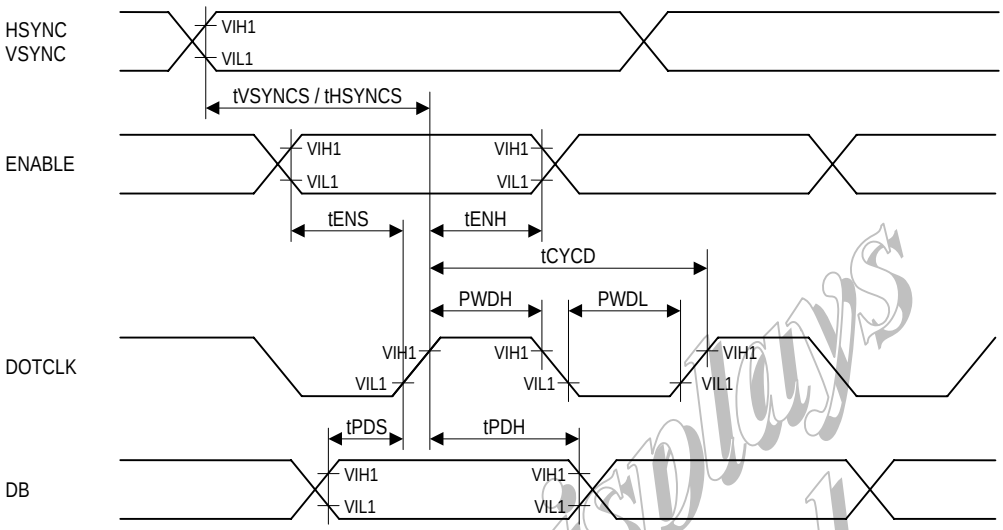


Figure 3: RGB interface timing

- Reset operation

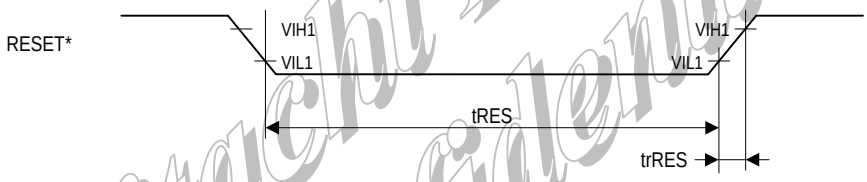


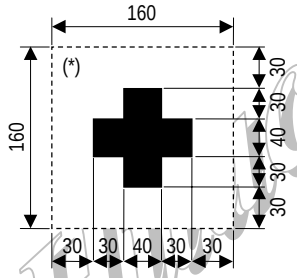
Figure 4: Reset operation timing

■ PAD layout

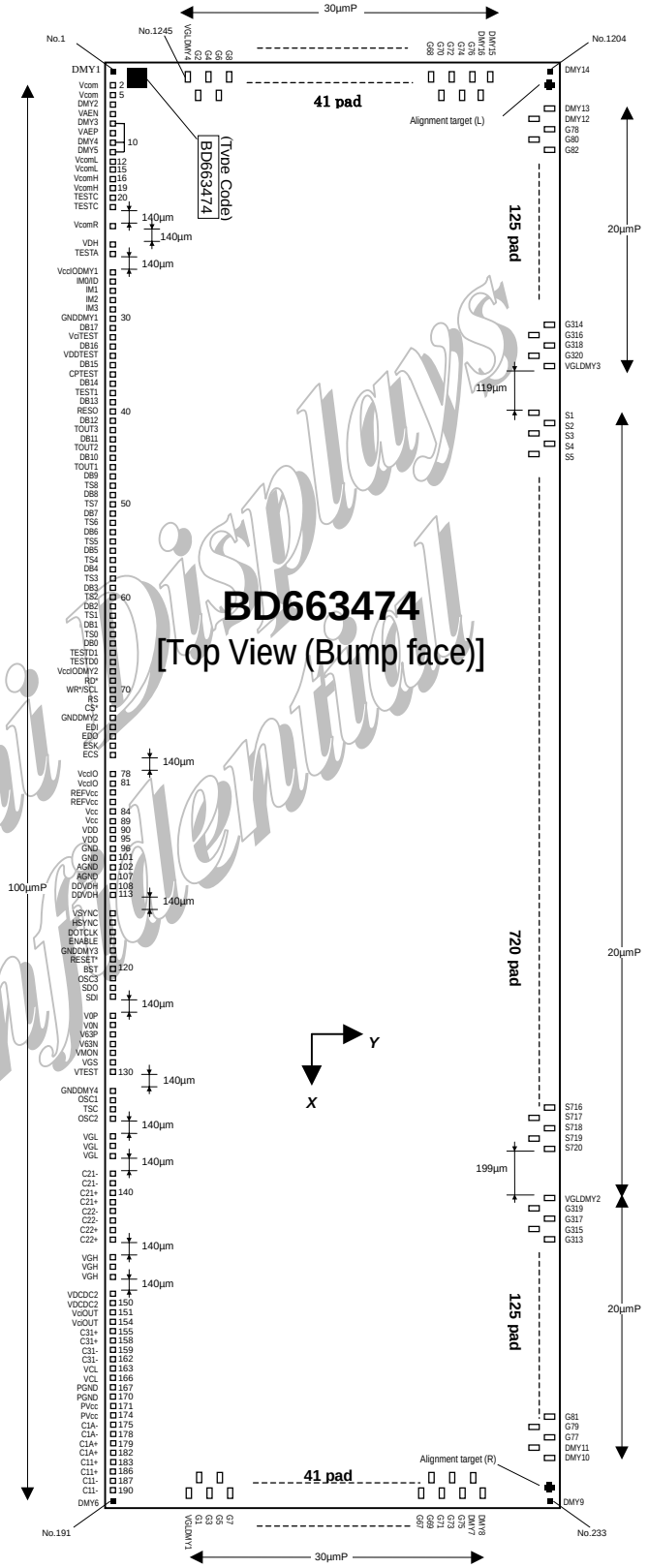
- Chip size : 20.5mm×2.15mm
- Chip thickness : 400µm (typ.)
- Pad coordinate : Pad center
- Origin of coordinate : Chip center
- Au bump size : As described below

1. 60µm×90µm
   Power supply pads and input pads
   (No.2~190)
2. 60µm×60µm
   Corner dummy pads
   (No.1, No.191, No.233, No.1204)
3. 100µm×26µm
   Driver output pads (left, right)
   (No.192~232, No.1205~1245)
4. 21µm×100µm
   Driver output pads (top)
   (No.234~1203)

- Au bump pitch : (See Figure on right)
- Au bump height: 15µm (typ.)
- Target for chip alignment (L, R)
  Pattern : Al (no gold bump provided)
  Size : See below. Origin of coordinates is at the center.



(*) : No pattern area



■ **Pad coordinates**

No.	Terminal name	X	Y
1	DMY1	-10135.0	-960.0
2	Vcom	-9920.0	-945.0
3	Vcom	-9820.0	-945.0
4	Vcom	-9720.0	-945.0
5	Vcom	-9620.0	-945.0
6	DMY2	-9520.0	-945.0
7	VAEN	-9420.0	-945.0
8	DMY3	-9320.0	-945.0
9	VAEP	-9220.0	-945.0
10	DMY4	-9120.0	-945.0
11	DMY5	-9020.0	-945.0
12	VcomL	-8920.0	-945.0
13	VcomL	-8820.0	-945.0
14	VcomL	-8720.0	-945.0
15	VcomL	-8620.0	-945.0
16	VcomH	-8520.0	-945.0
17	VcomH	-8420.0	-945.0
18	VcomH	-8320.0	-945.0
19	VcomH	-8220.0	-945.0
20	TESTC	-8120.0	-945.0
21	TESTC	-8020.0	-945.0
22	VcomR	-7820.0	-945.0
23	VDH	-7620.0	-945.0
24	TESTA	-7520.0	-945.0
25	VcclODMY1	-7320.0	-945.0
26	IM0/ID	-7220.0	-945.0
27	IM1	-7120.0	-945.0
28	IM2	-7020.0	-945.0
29	IM3	-6920.0	-945.0
30	GNDDMY1	-6820.0	-945.0
31	DB17	-6720.0	-945.0
32	VciTEST	-6620.0	-945.0
33	DB16	-6520.0	-945.0
34	VDDTEST	-6420.0	-945.0
35	DB15	-6320.0	-945.0
36	CPTEST	-6220.0	-945.0
37	DB14	-6120.0	-945.0
38	TEST1	-6020.0	-945.0
39	DB13	-5920.0	-945.0
40	RESO	-5820.0	-945.0
41	DB12	-5720.0	-945.0
42	TOUT3	-5620.0	-945.0
43	DB11	-5520.0	-945.0
44	TOUT2	-5420.0	-945.0
45	DB10	-5320.0	-945.0
46	TOUT1	-5220.0	-945.0
47	DB9	-5120.0	-945.0
48	TS8	-5020.0	-945.0
49	DB8	-4920.0	-945.0
50	TS7	-4820.0	-945.0
51	DB7	-4720.0	-945.0
52	TS6	-4620.0	-945.0
53	DB6	-4520.0	-945.0
54	TS5	-4420.0	-945.0
55	DB5	-4320.0	-945.0
56	TS4	-4220.0	-945.0
57	DB4	-4120.0	-945.0
58	TS3	-4020.0	-945.0
59	DB3	-3920.0	-945.0
60	TS2	-3820.0	-945.0
61	DB2	-3720.0	-945.0
62	TS1	-3620.0	-945.0
63	DB1	-3520.0	-945.0
64	TS0	-3420.0	-945.0
65	DB0	-3320.0	-945.0
66	TESTD1	-3220.0	-945.0
67	TESTD0	-3120.0	-945.0
68	VcclODMY2	-3020.0	-945.0
69	RD*	-2920.0	-945.0
70	WR*/SCL	-2820.0	-945.0
71	RS	-2720.0	-945.0
72	CS*	-2620.0	-945.0
73	GNDDMY2	-2520.0	-945.0
74	EDI	-2420.0	-945.0
75	EDO	-2320.0	-945.0
76	ESK	-2220.0	-945.0
77	ECS	-2120.0	-945.0
78	VccIO	-1920.0	-945.0
79	VccIO	-1820.0	-945.0
80	VccIO	-1720.0	-945.0
81	VccIO	-1620.0	-945.0
82	REFVcc	-1520.0	-945.0
83	REFVcc	-1420.0	-945.0
84	Vcc	-1320.0	-945.0
85	Vcc	-1220.0	-945.0
86	Vcc	-1120.0	-945.0
87	Vcc	-1020.0	-945.0
88	Vcc	-920.0	-945.0
89	Vcc	-820.0	-945.0
90	VDD	-720.0	-945.0
91	VDD	-620.0	-945.0
92	VDD	-520.0	-945.0
93	VDD	-420.0	-945.0
94	VDD	-320.0	-945.0
95	VDD	-220.0	-945.0
96	GND	-120.0	-945.0
97	GND	-20.0	-945.0
98	GND	80.0	-945.0
99	GND	180.0	-945.0
100	GND	280.0	-945.0
101	GND	380.0	-945.0
102	AGND	480.0	-945.0
103	AGND	580.0	-945.0
104	AGND	680.0	-945.0
105	AGND	780.0	-945.0
106	AGND	880.0	-945.0
107	AGND	980.0	-945.0
108	DDVDH	1080.0	-945.0
109	DDVDH	1180.0	-945.0
110	DDVDH	1280.0	-945.0
111	DDVDH	1380.0	-945.0
112	DDVDH	1480.0	-945.0
113	DDVDH	1580.0	-945.0
114	VSYNC	1780.0	-945.0
115	HSYNC	1880.0	-945.0
116	DOTCLK	1980.0	-945.0
117	ENABLE	2080.0	-945.0
118	GNDDMY3	2180.0	-945.0
119	RESET*	2280.0	-945.0
120	BST	2380.0	-945.0
121	OSC3	2480.0	-945.0
122	SDO	2580.0	-945.0
123	SDI	2680.0	-945.0
124	V0P	2880.0	-945.0
125	V0N	2980.0	-945.0
126	V63P	3080.0	-945.0
127	V63N	3180.0	-945.0
128	VMON	3280.0	-945.0
129	VGS	3380.0	-945.0
130	VTEST	3480.0	-945.0
131	GNDDMY4	3680.0	-945.0
132	OSC1	3780.0	-945.0
133	TSC	3880.0	-945.0
134	OSC2	3980.0	-945.0
135	VGL	4180.0	-945.0
136	VGL	4280.0	-945.0
137	VGL	4380.0	-945.0
138	C21-	4580.0	-945.0
139	C21-	4680.0	-945.0
140	C21+	4780.0	-945.0
141	C21+	4880.0	-945.0
142	C22-	4980.0	-945.0
143	C22-	5080.0	-945.0
144	C22+	5180.0	-945.0
145	C22+	5280.0	-945.0
146	VGH	5480.0	-945.0
147	VGH	5580.0	-945.0
148	VGH	5680.0	-945.0
149	VDCDC2	5880.0	-945.0
150	VDCDC2	5980.0	-945.0
151	VciOUT	6080.0	-945.0
152	VciOUT	6180.0	-945.0
153	VciOUT	6280.0	-945.0
154	VciOUT	6380.0	-945.0
155	C31+	6480.0	-945.0
156	C31+	6580.0	-945.0
157	C31+	6680.0	-945.0
158	C31+	6780.0	-945.0
159	C31-	6880.0	-945.0
160	C31-	6980.0	-945.0
161	C31-	7080.0	-945.0
162	C31-	7180.0	-945.0
163	VCL	7280.0	-945.0
164	VCL	7380.0	-945.0
165	VCL	7480.0	-945.0
166	VCL	7580.0	-945.0
167	PGND	7680.0	-945.0
168	PGND	7780.0	-945.0
169	PGND	7880.0	-945.0
170	PGND	7980.0	-945.0
171	PVcc	8080.0	-945.0
172	PVcc	8180.0	-945.0
173	PVcc	8280.0	-945.0
174	PVcc	8380.0	-945.0
175	C1A-	8480.0	-945.0
176	C1A-	8580.0	-945.0
177	C1A-	8680.0	-945.0
178	C1A-	8780.0	-945.0
179	C1A+	8880.0	-945.0
180	C1A+	8980.0	-945.0
181	C1A+	9080.0	-945.0
182	C1A+	9180.0	-945.0
183	C11+	9280.0	-945.0
184	C11+	9380.0	-945.0
185	C11+	9480.0	-945.0
186	C11+	9580.0	-945.0
187	C11-	9680.0	-945.0
188	C11-	9780.0	-945.0
189	C11-	9880.0	-945.0
190	C11-	9980.0	-945.0
191	DMY6	10135.0	-960.0
192	VGLDMY1	10115.0	-625.0
193	G1	9990.0	-595.0
194	G3	10115.0	-565.0
195	G5	9990.0	-535.0

No.	Terminal name	X	Y
196	G7	10115.0	-505.0
197	G9	9990.0	-475.0
198	G11	10115.0	-445.0
199	G13	9990.0	-415.0
200	G15	10115.0	-385.0
201	G17	9990.0	-355.0
202	G19	10115.0	-325.0
203	G21	9990.0	-295.0
204	G23	10115.0	-265.0
205	G25	9990.0	-235.0
206	G27	10115.0	-205.0
207	G29	9990.0	-175.0
208	G31	10115.0	-145.0
209	G33	9990.0	-115.0
210	G35	10115.0	-85.0
211	G37	9990.0	-55.0
212	G39	10115.0	-25.0
213	G41	9990.0	5.0
214	G43	10115.0	35.0
215	G45	9990.0	65.0
216	G47	10115.0	95.0
217	G49	9990.0	125.0
218	G51	10115.0	155.0
219	G53	9990.0	185.0
220	G55	10115.0	215.0
221	G57	9990.0	245.0
222	G59	10115.0	275.0
223	G61	9990.0	305.0
224	G63	10115.0	335.0
225	G65	9990.0	365.0
226	G67	10115.0	395.0
227	G69	9990.0	425.0
228	G71	10115.0	455.0
229	G73	9990.0	485.0
230	G75	10115.0	515.0
231	DMY7	9990.0	545.0
232	DMY8	10115.0	575.0
233	DMY9	10135.0	960.0
234	DMY10	9850.0	940.0
235	DMY11	9830.0	815.0
236	G77	9810.0	940.0
237	G79	9790.0	815.0
238	G81	9770.0	940.0
239	G83	9750.0	815.0
240	G85	9730.0	940.0
241	G87	9710.0	815.0
242	G89	9690.0	940.0
243	G91	9670.0	815.0
244	G93	9650.0	940.0
245	G95	9630.0	815.0
246	G97	9610.0	940.0
247	G99	9590.0	815.0
248	G101	9570.0	940.0
249	G103	9550.0	815.0
250	G105	9530.0	940.0
251	G107	9510.0	815.0
252	G109	9490.0	940.0
253	G111	9470.0	815.0
254	G113	9450.0	940.0
255	G115	9430.0	815.0
256	G117	9410.0	940.0
257	G119	9390.0	815.0
258	G121	9370.0	940.0
259	G123	9350.0	815.0
260	G125	9330.0	940.0

No.	Terminal name	X	Y
261	G127	9310.0	815.0
262	G129	9290.0	940.0
263	G131	9270.0	815.0
264	G133	9250.0	940.0
265	G135	9230.0	815.0
266	G137	9210.0	940.0
267	G139	9190.0	815.0
268	G141	9170.0	940.0
269	G143	9150.0	815.0
270	G145	9130.0	940.0
271	G147	9110.0	815.0
272	G149	9090.0	940.0
273	G151	9070.0	815.0
274	G153	9050.0	940.0
275	G155	9030.0	815.0
276	G157	9010.0	940.0
277	G159	8990.0	815.0
278	G161	8970.0	940.0
279	G163	8950.0	815.0
280	G165	8930.0	940.0
281	G167	8910.0	815.0
282	G169	8890.0	940.0
283	G171	8870.0	815.0
284	G173	8850.0	940.0
285	G175	8830.0	815.0
286	G177	8810.0	940.0
287	G179	8790.0	815.0
288	G181	8770.0	940.0
289	G183	8750.0	815.0
290	G185	8730.0	940.0
291	G187	8710.0	815.0
292	G189	8690.0	940.0
293	G191	8670.0	815.0
294	G193	8650.0	940.0
295	G195	8630.0	815.0
296	G197	8610.0	940.0
297	G199	8590.0	815.0
298	G201	8570.0	940.0
299	G203	8550.0	815.0
300	G205	8530.0	940.0
301	G207	8510.0	815.0
302	G209	8490.0	940.0
303	G211	8470.0	815.0
304	G213	8450.0	940.0
305	G215	8430.0	815.0
306	G217	8410.0	940.0
307	G219	8390.0	815.0
308	G221	8370.0	940.0
309	G223	8350.0	815.0
310	G225	8330.0	940.0
311	G227	8310.0	815.0
312	G229	8290.0	940.0
313	G231	8270.0	815.0
314	G233	8250.0	940.0
315	G235	8230.0	815.0
316	G237	8210.0	940.0
317	G239	8190.0	815.0
318	G241	8170.0	940.0
319	G243	8150.0	815.0
320	G245	8130.0	940.0
321	G247	8110.0	815.0
322	G249	8090.0	940.0
323	G251	8070.0	815.0
324	G253	8050.0	940.0
325	G255	8030.0	815.0

No.	Terminal name	X	Y
326	G257	8010.0	940.0
327	G259	7990.0	815.0
328	G261	7970.0	940.0
329	G263	7950.0	815.0
330	G265	7930.0	940.0
331	G267	7910.0	815.0
332	G269	7890.0	940.0
333	G271	7870.0	815.0
334	G273	7850.0	940.0
335	G275	7830.0	815.0
336	G277	7810.0	940.0
337	G279	7790.0	815.0
338	G281	7770.0	940.0
339	G283	7750.0	815.0
340	G285	7730.0	940.0
341	G287	7710.0	815.0
342	G289	7690.0	940.0
343	G291	7670.0	815.0
344	G293	7650.0	940.0
345	G295	7630.0	815.0
346	G297	7610.0	940.0
347	G299	7590.0	815.0
348	G301	7570.0	940.0
349	G303	7550.0	815.0
350	G305	7530.0	940.0
351	G307	7510.0	815.0
352	G309	7490.0	940.0
353	G311	7470.0	815.0
354	G313	7450.0	940.0
355	G315	7430.0	815.0
356	G317	7410.0	940.0
357	G319	7390.0	815.0
358	VGLDMY2	7370.0	940.0
359	S720	7150.0	940.0
360	S719	7130.0	815.0
361	S718	7110.0	940.0
362	S717	7090.0	815.0
363	S716	7070.0	940.0
364	S715	7050.0	815.0
365	S714	7030.0	940.0
366	S713	7010.0	815.0
367	S712	6990.0	940.0
368	S711	6970.0	815.0
369	S710	6950.0	940.0
370	S709	6930.0	815.0
371	S708	6910.0	940.0
372	S707	6890.0	815.0
373	S706	6870.0	940.0
374	S705	6850.0	815.0
375	S704	6830.0	940.0
376	S703	6810.0	815.0
377	S702	6790.0	940.0
378	S701	6770.0	815.0
379	S700	6750.0	940.0
380	S699	6730.0	815.0
381	S698	6710.0	940.0
382	S697	6690.0	815.0
383	S696	6670.0	940.0
384	S695	6650.0	815.0
385	S694	6630.0	940.0
386	S693	6610.0	815.0
387	S692	6590.0	940.0
388	S691	6570.0	815.0
389	S690	6550.0	940.0
390	S689	6530.0	815.0

No.	Terminal name	X	Y
391	S688	6510.0	940.0
392	S687	6490.0	815.0
393	S686	6470.0	940.0
394	S685	6450.0	815.0
395	S684	6430.0	940.0
396	S683	6410.0	815.0
397	S682	6390.0	940.0
398	S681	6370.0	815.0
399	S680	6350.0	940.0
400	S679	6330.0	815.0
401	S678	6310.0	940.0
402	S677	6290.0	815.0
403	S676	6270.0	940.0
404	S675	6250.0	815.0
405	S674	6230.0	940.0
406	S673	6210.0	815.0
407	S672	6190.0	940.0
408	S671	6170.0	815.0
409	S670	6150.0	940.0
410	S669	6130.0	815.0
411	S668	6110.0	940.0
412	S667	6090.0	815.0
413	S666	6070.0	940.0
414	S665	6050.0	815.0
415	S664	6030.0	940.0
416	S663	6010.0	815.0
417	S662	5990.0	940.0
418	S661	5970.0	815.0
419	S660	5950.0	940.0
420	S659	5930.0	815.0
421	S658	5910.0	940.0
422	S657	5890.0	815.0
423	S656	5870.0	940.0
424	S655	5850.0	815.0
425	S654	5830.0	940.0
426	S653	5810.0	815.0
427	S652	5790.0	940.0
428	S651	5770.0	815.0
429	S650	5750.0	940.0
430	S649	5730.0	815.0
431	S648	5710.0	940.0
432	S647	5690.0	815.0
433	S646	5670.0	940.0
434	S645	5650.0	815.0
435	S644	5630.0	940.0
436	S643	5610.0	815.0
437	S642	5590.0	940.0
438	S641	5570.0	815.0
439	S640	5550.0	940.0
440	S639	5530.0	815.0
441	S638	5510.0	940.0
442	S637	5490.0	815.0
443	S636	5470.0	940.0
444	S635	5450.0	815.0
445	S634	5430.0	940.0
446	S633	5410.0	815.0
447	S632	5390.0	940.0
448	S631	5370.0	815.0
449	S630	5350.0	940.0
450	S629	5330.0	815.0
451	S628	5310.0	940.0
452	S627	5290.0	815.0
453	S626	5270.0	940.0
454	S625	5250.0	815.0
455	S624	5230.0	940.0
456	S623	5210.0	815.0
457	S622	5190.0	940.0
458	S621	5170.0	815.0
459	S620	5150.0	940.0
460	S619	5130.0	815.0
461	S618	5110.0	940.0
462	S617	5090.0	815.0
463	S616	5070.0	940.0
464	S615	5050.0	815.0
465	S614	5030.0	940.0
466	S613	5010.0	815.0
467	S612	4990.0	940.0
468	S611	4970.0	815.0
469	S610	4950.0	940.0
470	S609	4930.0	815.0
471	S608	4910.0	940.0
472	S607	4890.0	815.0
473	S606	4870.0	940.0
474	S605	4850.0	815.0
475	S604	4830.0	940.0
476	S603	4810.0	815.0
477	S602	4790.0	940.0
478	S601	4770.0	815.0
479	S600	4750.0	940.0
480	S599	4730.0	815.0
481	S598	4710.0	940.0
482	S597	4690.0	815.0
483	S596	4670.0	940.0
484	S595	4650.0	815.0
485	S594	4630.0	940.0
486	S593	4610.0	815.0
487	S592	4590.0	940.0
488	S591	4570.0	815.0
489	S590	4550.0	940.0
490	S589	4530.0	815.0
491	S588	4510.0	940.0
492	S587	4490.0	815.0
493	S586	4470.0	940.0
494	S585	4450.0	815.0
495	S584	4430.0	940.0
496	S583	4410.0	815.0
497	S582	4390.0	940.0
498	S581	4370.0	815.0
499	S580	4350.0	940.0
500	S579	4330.0	815.0
501	S578	4310.0	940.0
502	S577	4290.0	815.0
503	S576	4270.0	940.0
504	S575	4250.0	815.0
505	S574	4230.0	940.0
506	S573	4210.0	815.0
507	S572	4190.0	940.0
508	S571	4170.0	815.0
509	S570	4150.0	940.0
510	S569	4130.0	815.0
511	S568	4110.0	940.0
512	S567	4090.0	815.0
513	S566	4070.0	940.0
514	S565	4050.0	815.0
515	S564	4030.0	940.0
516	S563	4010.0	815.0
517	S562	3990.0	940.0
518	S561	3970.0	815.0
519	S560	3950.0	940.0
520	S559	3930.0	815.0
521	S558	3910.0	940.0
522	S557	3890.0	815.0
523	S556	3870.0	940.0
524	S555	3850.0	815.0
525	S554	3830.0	940.0
526	S553	3810.0	815.0
527	S552	3790.0	940.0
528	S551	3770.0	815.0
529	S550	3750.0	940.0
530	S549	3730.0	815.0
531	S548	3710.0	940.0
532	S547	3690.0	815.0
533	S546	3670.0	940.0
534	S545	3650.0	815.0
535	S544	3630.0	940.0
536	S543	3610.0	815.0
537	S542	3590.0	940.0
538	S541	3570.0	815.0
539	S540	3550.0	940.0
540	S539	3530.0	815.0
541	S538	3510.0	940.0
542	S537	3490.0	815.0
543	S536	3470.0	940.0
544	S535	3450.0	815.0
545	S534	3430.0	940.0
546	S533	3410.0	815.0
547	S532	3390.0	940.0
548	S531	3370.0	815.0
549	S530	3350.0	940.0
550	S529	3330.0	815.0
551	S528	3310.0	940.0
552	S527	3290.0	815.0
553	S526	3270.0	940.0
554	S525	3250.0	815.0
555	S524	3230.0	940.0
556	S523	3210.0	815.0
557	S522	3190.0	940.0
558	S521	3170.0	815.0
559	S520	3150.0	940.0
560	S519	3130.0	815.0
561	S518	3110.0	940.0
562	S517	3090.0	815.0
563	S516	3070.0	940.0
564	S515	3050.0	815.0
565	S514	3030.0	940.0
566	S513	3010.0	815.0
567	S512	2990.0	940.0
568	S511	2970.0	815.0
569	S510	2950.0	940.0
570	S509	2930.0	815.0
571	S508	2910.0	940.0
572	S507	2890.0	815.0
573	S506	2870.0	940.0
574	S505	2850.0	815.0
575	S504	2830.0	940.0
576	S503	2810.0	815.0
577	S502	2790.0	940.0
578	S501	2770.0	815.0
579	S500	2750.0	940.0
580	S499	2730.0	815.0
581	S498	2710.0	940.0
582	S497	2690.0	815.0
583	S496	2670.0	940.0
584	S495	2650.0	815.0
585	S494	2630.0	940.0

No.	Terminal name	X	Y
586	S493	2610.0	815.0
587	S492	2590.0	940.0
588	S491	2570.0	815.0
589	S490	2550.0	940.0
590	S489	2530.0	815.0
591	S488	2510.0	940.0
592	S487	2490.0	815.0
593	S486	2470.0	940.0
594	S485	2450.0	815.0
595	S484	2430.0	940.0
596	S483	2410.0	815.0
597	S482	2390.0	940.0
598	S481	2370.0	815.0
599	S480	2350.0	940.0
600	S479	2330.0	815.0
601	S478	2310.0	940.0
602	S477	2290.0	815.0
603	S476	2270.0	940.0
604	S475	2250.0	815.0
605	S474	2230.0	940.0
606	S473	2210.0	815.0
607	S472	2190.0	940.0
608	S471	2170.0	815.0
609	S470	2150.0	940.0
610	S469	2130.0	815.0
611	S468	2110.0	940.0
612	S467	2090.0	815.0
613	S466	2070.0	940.0
614	S465	2050.0	815.0
615	S464	2030.0	940.0
616	S463	2010.0	815.0
617	S462	1990.0	940.0
618	S461	1970.0	815.0
619	S460	1950.0	940.0
620	S459	1930.0	815.0
621	S458	1910.0	940.0
622	S457	1890.0	815.0
623	S456	1870.0	940.0
624	S455	1850.0	815.0
625	S454	1830.0	940.0
626	S453	1810.0	815.0
627	S452	1790.0	940.0
628	S451	1770.0	815.0
629	S450	1750.0	940.0
630	S449	1730.0	815.0
631	S448	1710.0	940.0
632	S447	1690.0	815.0
633	S446	1670.0	940.0
634	S445	1650.0	815.0
635	S444	1630.0	940.0
636	S443	1610.0	815.0
637	S442	1590.0	940.0
638	S441	1570.0	815.0
639	S440	1550.0	940.0
640	S439	1530.0	815.0
641	S438	1510.0	940.0
642	S437	1490.0	815.0
643	S436	1470.0	940.0
644	S435	1450.0	815.0
645	S434	1430.0	940.0
646	S433	1410.0	815.0
647	S432	1390.0	940.0
648	S431	1370.0	815.0
649	S430	1350.0	940.0
650	S429	1330.0	815.0

No.	Terminal name	X	Y
651	S428	1310.0	940.0
652	S427	1290.0	815.0
653	S426	1270.0	940.0
654	S425	1250.0	815.0
655	S424	1230.0	940.0
656	S423	1210.0	815.0
657	S422	1190.0	940.0
658	S421	1170.0	815.0
659	S420	1150.0	940.0
660	S419	1130.0	815.0
661	S418	1110.0	940.0
662	S417	1090.0	815.0
663	S416	1070.0	940.0
664	S415	1050.0	815.0
665	S414	1030.0	940.0
666	S413	1010.0	815.0
667	S412	990.0	940.0
668	S411	970.0	815.0
669	S410	950.0	940.0
670	S409	930.0	815.0
671	S408	910.0	940.0
672	S407	890.0	815.0
673	S406	870.0	940.0
674	S405	850.0	815.0
675	S404	830.0	940.0
676	S403	810.0	815.0
677	S402	790.0	940.0
678	S401	770.0	815.0
679	S400	750.0	940.0
680	S399	730.0	815.0
681	S398	710.0	940.0
682	S397	690.0	815.0
683	S396	670.0	940.0
684	S395	650.0	815.0
685	S394	630.0	940.0
686	S393	610.0	815.0
687	S392	590.0	940.0
688	S391	570.0	815.0
689	S390	550.0	940.0
690	S389	530.0	815.0
691	S388	510.0	940.0
692	S387	490.0	815.0
693	S386	470.0	940.0
694	S385	450.0	815.0
695	S384	430.0	940.0
696	S383	410.0	815.0
697	S382	390.0	940.0
698	S381	370.0	815.0
699	S380	350.0	940.0
700	S379	330.0	815.0
701	S378	310.0	940.0
702	S377	290.0	815.0
703	S376	270.0	940.0
704	S375	250.0	815.0
705	S374	230.0	940.0
706	S373	210.0	815.0
707	S372	190.0	940.0
708	S371	170.0	815.0
709	S370	150.0	940.0
710	S369	130.0	815.0
711	S368	110.0	940.0
712	S367	90.0	815.0
713	S366	70.0	940.0
714	S365	50.0	815.0
715	S364	30.0	940.0

No.	Terminal name	X	Y
716	S363	10.0	815.0
717	S362	-10.0	940.0
718	S361	-30.0	815.0
719	S360	-50.0	940.0
720	S359	-70.0	815.0
721	S358	-90.0	940.0
722	S357	-110.0	815.0
723	S356	-130.0	940.0
724	S355	-150.0	815.0
725	S354	-170.0	940.0
726	S353	-190.0	815.0
727	S352	-210.0	940.0
728	S351	-230.0	815.0
729	S350	-250.0	940.0
730	S349	-270.0	815.0
731	S348	-290.0	940.0
732	S347	-310.0	815.0
733	S346	-330.0	940.0
734	S345	-350.0	815.0
735	S344	-370.0	940.0
736	S343	-390.0	815.0
737	S342	-410.0	940.0
738	S341	-430.0	815.0
739	S340	-450.0	940.0
740	S339	-470.0	815.0
741	S338	-490.0	940.0
742	S337	-510.0	815.0
743	S336	-530.0	940.0
744	S335	-550.0	815.0
745	S334	-570.0	940.0
746	S333	-590.0	815.0
747	S332	-610.0	940.0
748	S331	-630.0	815.0
749	S330	-650.0	940.0
750	S329	-670.0	815.0
751	S328	-690.0	940.0
752	S327	-710.0	815.0
753	S326	-730.0	940.0
754	S325	-750.0	815.0
755	S324	-770.0	940.0
756	S323	-790.0	815.0
757	S322	-810.0	940.0
758	S321	-830.0	815.0
759	S320	-850.0	940.0
760	S319	-870.0	815.0
761	S318	-890.0	940.0
762	S317	-910.0	815.0
763	S316	-930.0	940.0
764	S315	-950.0	815.0
765	S314	-970.0	940.0
766	S313	-990.0	815.0
767	S312	-1010.0	940.0
768	S311	-1030.0	815.0
769	S310	-1050.0	940.0
770	S309	-1070.0	815.0
771	S308	-1090.0	940.0
772	S307	-1110.0	815.0
773	S306	-1130.0	940.0
774	S305	-1150.0	815.0
775	S304	-1170.0	940.0
776	S303	-1190.0	815.0
777	S302	-1210.0	940.0
778	S301	-1230.0	815.0
779	S300	-1250.0	940.0
780	S299	-1270.0	815.0

No.	Terminal name	X	Y
781	S298	-1290.0	940.0
782	S297	-1310.0	815.0
783	S296	-1330.0	940.0
784	S295	-1350.0	815.0
785	S294	-1370.0	940.0
786	S293	-1390.0	815.0
787	S292	-1410.0	940.0
788	S291	-1430.0	815.0
789	S290	-1450.0	940.0
790	S289	-1470.0	815.0
791	S288	-1490.0	940.0
792	S287	-1510.0	815.0
793	S286	-1530.0	940.0
794	S285	-1550.0	815.0
795	S284	-1570.0	940.0
796	S283	-1590.0	815.0
797	S282	-1610.0	940.0
798	S281	-1630.0	815.0
799	S280	-1650.0	940.0
800	S279	-1670.0	815.0
801	S278	-1690.0	940.0
802	S277	-1710.0	815.0
803	S276	-1730.0	940.0
804	S275	-1750.0	815.0
805	S274	-1770.0	940.0
806	S273	-1790.0	815.0
807	S272	-1810.0	940.0
808	S271	-1830.0	815.0
809	S270	-1850.0	940.0
810	S269	-1870.0	815.0
811	S268	-1890.0	940.0
812	S267	-1910.0	815.0
813	S266	-1930.0	940.0
814	S265	-1950.0	815.0
815	S264	-1970.0	940.0
816	S263	-1990.0	815.0
817	S262	-2010.0	940.0
818	S261	-2030.0	815.0
819	S260	-2050.0	940.0
820	S259	-2070.0	815.0
821	S258	-2090.0	940.0
822	S257	-2110.0	815.0
823	S256	-2130.0	940.0
824	S255	-2150.0	815.0
825	S254	-2170.0	940.0
826	S253	-2190.0	815.0
827	S252	-2210.0	940.0
828	S251	-2230.0	815.0
829	S250	-2250.0	940.0
830	S249	-2270.0	815.0
831	S248	-2290.0	940.0
832	S247	-2310.0	815.0
833	S246	-2330.0	940.0
834	S245	-2350.0	815.0
835	S244	-2370.0	940.0
836	S243	-2390.0	815.0
837	S242	-2410.0	940.0
838	S241	-2430.0	815.0
839	S240	-2450.0	940.0
840	S239	-2470.0	815.0
841	S238	-2490.0	940.0
842	S237	-2510.0	815.0
843	S236	-2530.0	940.0
844	S235	-2550.0	815.0
845	S234	-2570.0	940.0

No.	Terminal name	X	Y
846	S233	-2590.0	815.0
847	S232	-2610.0	940.0
848	S231	-2630.0	815.0
849	S230	-2650.0	940.0
850	S229	-2670.0	815.0
851	S228	-2690.0	940.0
852	S227	-2710.0	815.0
853	S226	-2730.0	940.0
854	S225	-2750.0	815.0
855	S224	-2770.0	940.0
856	S223	-2790.0	815.0
857	S222	-2810.0	940.0
858	S221	-2830.0	815.0
859	S220	-2850.0	940.0
860	S219	-2870.0	815.0
861	S218	-2890.0	940.0
862	S217	-2910.0	815.0
863	S216	-2930.0	940.0
864	S215	-2950.0	815.0
865	S214	-2970.0	940.0
866	S213	-2990.0	815.0
867	S212	-3010.0	940.0
868	S211	-3030.0	815.0
869	S210	-3050.0	940.0
870	S209	-3070.0	815.0
871	S208	-3090.0	940.0
872	S207	-3110.0	815.0
873	S206	-3130.0	940.0
874	S205	-3150.0	815.0
875	S204	-3170.0	940.0
876	S203	-3190.0	815.0
877	S202	-3210.0	940.0
878	S201	-3230.0	815.0
879	S200	-3250.0	940.0
880	S199	-3270.0	815.0
881	S198	-3290.0	940.0
882	S197	-3310.0	815.0
883	S196	-3330.0	940.0
884	S195	-3350.0	815.0
885	S194	-3370.0	940.0
886	S193	-3390.0	815.0
887	S192	-3410.0	940.0
888	S191	-3430.0	815.0
889	S190	-3450.0	940.0
890	S189	-3470.0	815.0
891	S188	-3490.0	940.0
892	S187	-3510.0	815.0
893	S186	-3530.0	940.0
894	S185	-3550.0	815.0
895	S184	-3570.0	940.0
896	S183	-3590.0	815.0
897	S182	-3610.0	940.0
898	S181	-3630.0	815.0
899	S180	-3650.0	940.0
900	S179	-3670.0	815.0
901	S178	-3690.0	940.0
902	S177	-3710.0	815.0
903	S176	-3730.0	940.0
904	S175	-3750.0	815.0
905	S174	-3770.0	940.0
906	S173	-3790.0	815.0
907	S172	-3810.0	940.0
908	S171	-3830.0	815.0
909	S170	-3850.0	940.0
910	S169	-3870.0	815.0

No.	Terminal name	X	Y
911	S168	-3890.0	940.0
912	S167	-3910.0	815.0
913	S166	-3930.0	940.0
914	S165	-3950.0	815.0
915	S164	-3970.0	940.0
916	S163	-3990.0	815.0
917	S162	-4010.0	940.0
918	S161	-4030.0	815.0
919	S160	-4050.0	940.0
920	S159	-4070.0	815.0
921	S158	-4090.0	940.0
922	S157	-4110.0	815.0
923	S156	-4130.0	940.0
924	S155	-4150.0	815.0
925	S154	-4170.0	940.0
926	S153	-4190.0	815.0
927	S152	-4210.0	940.0
928	S151	-4230.0	815.0
929	S150	-4250.0	940.0
930	S149	-4270.0	815.0
931	S148	-4290.0	940.0
932	S147	-4310.0	815.0
933	S146	-4330.0	940.0
934	S145	-4350.0	815.0
935	S144	-4370.0	940.0
936	S143	-4390.0	815.0
937	S142	-4410.0	940.0
938	S141	-4430.0	815.0
939	S140	-4450.0	940.0
940	S139	-4470.0	815.0
941	S138	-4490.0	940.0
942	S137	-4510.0	815.0
943	S136	-4530.0	940.0
944	S135	-4550.0	815.0
945	S134	-4570.0	940.0
946	S133	-4590.0	815.0
947	S132	-4610.0	940.0
948	S131	-4630.0	815.0
949	S130	-4650.0	940.0
950	S129	-4670.0	815.0
951	S128	-4690.0	940.0
952	S127	-4710.0	815.0
953	S126	-4730.0	940.0
954	S125	-4750.0	815.0
955	S124	-4770.0	940.0
956	S123	-4790.0	815.0
957	S122	-4810.0	940.0
958	S121	-4830.0	815.0
959	S120	-4850.0	940.0
960	S119	-4870.0	815.0
961	S118	-4890.0	940.0
962	S117	-4910.0	815.0
963	S116	-4930.0	940.0
964	S115	-4950.0	815.0
965	S114	-4970.0	940.0
966	S113	-4990.0	815.0
967	S112	-5010.0	940.0
968	S111	-5030.0	815.0
969	S110	-5050.0	940.0
970	S109	-5070.0	815.0
971	S108	-5090.0	940.0
972	S107	-5110.0	815.0
973	S106	-5130.0	940.0
974	S105	-5150.0	815.0
975	S104	-5170.0	940.0

No.	Terminal name	X	Y
976	S103	-5190.0	815.0
977	S102	-5210.0	940.0
978	S101	-5230.0	815.0
979	S100	-5250.0	940.0
980	S99	-5270.0	815.0
981	S98	-5290.0	940.0
982	S97	-5310.0	815.0
983	S96	-5330.0	940.0
984	S95	-5350.0	815.0
985	S94	-5370.0	940.0
986	S93	-5390.0	815.0
987	S92	-5410.0	940.0
988	S91	-5430.0	815.0
989	S90	-5450.0	940.0
990	S89	-5470.0	815.0
991	S88	-5490.0	940.0
992	S87	-5510.0	815.0
993	S86	-5530.0	940.0
994	S85	-5550.0	815.0
995	S84	-5570.0	940.0
996	S83	-5590.0	815.0
997	S82	-5610.0	940.0
998	S81	-5630.0	815.0
999	S80	-5650.0	940.0
1000	S79	-5670.0	815.0
1001	S78	-5690.0	940.0
1002	S77	-5710.0	815.0
1003	S76	-5730.0	940.0
1004	S75	-5750.0	815.0
1005	S74	-5770.0	940.0
1006	S73	-5790.0	815.0
1007	S72	-5810.0	940.0
1008	S71	-5830.0	815.0
1009	S70	-5850.0	940.0
1010	S69	-5870.0	815.0
1011	S68	-5890.0	940.0
1012	S67	-5910.0	815.0
1013	S66	-5930.0	940.0
1014	S65	-5950.0	815.0
1015	S64	-5970.0	940.0
1016	S63	-5990.0	815.0
1017	S62	-6010.0	940.0
1018	S61	-6030.0	815.0
1019	S60	-6050.0	940.0
1020	S59	-6070.0	815.0
1021	S58	-6090.0	940.0
1022	S57	-6110.0	815.0
1023	S56	-6130.0	940.0
1024	S55	-6150.0	815.0
1025	S54	-6170.0	940.0
1026	S53	-6190.0	815.0
1027	S52	-6210.0	940.0
1028	S51	-6230.0	815.0
1029	S50	-6250.0	940.0
1030	S49	-6270.0	815.0
1031	S48	-6290.0	940.0
1032	S47	-6310.0	815.0
1033	S46	-6330.0	940.0
1034	S45	-6350.0	815.0
1035	S44	-6370.0	940.0
1036	S43	-6390.0	815.0
1037	S42	-6410.0	940.0
1038	S41	-6430.0	815.0
1039	S40	-6450.0	940.0
1040	S39	-6470.0	815.0
1041	S38	-6490.0	940.0
1042	S37	-6510.0	815.0
1043	S36	-6530.0	940.0
1044	S35	-6550.0	815.0
1045	S34	-6570.0	940.0
1046	S33	-6590.0	815.0
1047	S32	-6610.0	940.0
1048	S31	-6630.0	815.0
1049	S30	-6650.0	940.0
1050	S29	-6670.0	815.0
1051	S28	-6690.0	940.0
1052	S27	-6710.0	815.0
1053	S26	-6730.0	940.0
1054	S25	-6750.0	815.0
1055	S24	-6770.0	940.0
1056	S23	-6790.0	815.0
1057	S22	-6810.0	940.0
1058	S21	-6830.0	815.0
1059	S20	-6850.0	940.0
1060	S19	-6870.0	815.0
1061	S18	-6890.0	940.0
1062	S17	-6910.0	815.0
1063	S16	-6930.0	940.0
1064	S15	-6950.0	815.0
1065	S14	-6970.0	940.0
1066	S13	-6990.0	815.0
1067	S12	-7010.0	940.0
1068	S11	-7030.0	815.0
1069	S10	-7050.0	940.0
1070	S9	-7070.0	815.0
1071	S8	-7090.0	940.0
1072	S7	-7110.0	815.0
1073	S6	-7130.0	940.0
1074	S5	-7150.0	815.0
1075	S4	-7170.0	940.0
1076	S3	-7190.0	815.0
1077	S2	-7210.0	940.0
1078	S1	-7230.0	815.0
1079	VGLDMY3	-7370.0	940.0
1080	G320	-7390.0	815.0
1081	G318	-7410.0	940.0
1082	G316	-7430.0	815.0
1083	G314	-7450.0	940.0
1084	G312	-7470.0	815.0
1085	G310	-7490.0	940.0
1086	G308	-7510.0	815.0
1087	G306	-7530.0	940.0
1088	G304	-7550.0	815.0
1089	G302	-7570.0	940.0
1090	G300	-7590.0	815.0
1091	G298	-7610.0	940.0
1092	G296	-7630.0	815.0
1093	G294	-7650.0	940.0
1094	G292	-7670.0	815.0
1095	G290	-7690.0	940.0
1096	G288	-7710.0	815.0
1097	G286	-7730.0	940.0
1098	G284	-7750.0	815.0
1099	G282	-7770.0	940.0
1100	G280	-7790.0	815.0
1101	G278	-7810.0	940.0
1102	G276	-7830.0	815.0
1103	G274	-7850.0	940.0
1104	G272	-7870.0	815.0
1105	G270	-7890.0	940.0
1106	G268	-7910.0	815.0
1107	G266	-7930.0	940.0
1108	G264	-7950.0	815.0
1109	G262	-7970.0	940.0
1110	G260	-7990.0	815.0
1111	G258	-8010.0	940.0
1112	G256	-8030.0	815.0
1113	G254	-8050.0	940.0
1114	G252	-8070.0	815.0
1115	G250	-8090.0	940.0
1116	G248	-8110.0	815.0
1117	G246	-8130.0	940.0
1118	G244	-8150.0	815.0
1119	G242	-8170.0	940.0
1120	G240	-8190.0	815.0
1121	G238	-8210.0	940.0
1122	G236	-8230.0	815.0
1123	G234	-8250.0	940.0
1124	G232	-8270.0	815.0
1125	G230	-8290.0	940.0
1126	G228	-8310.0	815.0
1127	G226	-8330.0	940.0
1128	G224	-8350.0	815.0
1129	G222	-8370.0	940.0
1130	G220	-8390.0	815.0
1131	G218	-8410.0	940.0
1132	G216	-8430.0	815.0
1133	G214	-8450.0	940.0
1134	G212	-8470.0	815.0
1135	G210	-8490.0	940.0
1136	G208	-8510.0	815.0
1137	G206	-8530.0	940.0
1138	G204	-8550.0	815.0
1139	G202	-8570.0	940.0
1140	G200	-8590.0	815.0
1141	G198	-8610.0	940.0
1142	G196	-8630.0	815.0
1143	G194	-8650.0	940.0
1144	G192	-8670.0	815.0
1145	G190	-8690.0	940.0
1146	G188	-8710.0	815.0
1147	G186	-8730.0	940.0
1148	G184	-8750.0	815.0
1149	G182	-8770.0	940.0
1150	G180	-8790.0	815.0
1151	G178	-8810.0	940.0
1152	G176	-8830.0	815.0
1153	G174	-8850.0	940.0
1154	G172	-8870.0	815.0
1155	G170	-8890.0	940.0
1156	G168	-8910.0	815.0
1157	G166	-8930.0	940.0
1158	G164	-8950.0	815.0
1159	G162	-8970.0	940.0
1160	G160	-8990.0	815.0
1161	G158	-9010.0	940.0
1162	G156	-9030.0	815.0
1163	G154	-9050.0	940.0
1164	G152	-9070.0	815.0
1165	G150	-9090.0	940.0
1166	G148	-9110.0	815.0
1167	G146	-9130.0	940.0
1168	G144	-9150.0	815.0
1169	G142	-9170.0	940.0
1170	G140	-9190.0	815.0

No.	Terminal name	X	Y
1171	G138	-9210.0	940.0
1172	G136	-9230.0	815.0
1173	G134	-9250.0	940.0
1174	G132	-9270.0	815.0
1175	G130	-9290.0	940.0
1176	G128	-9310.0	815.0
1177	G126	-9330.0	940.0
1178	G124	-9350.0	815.0
1179	G122	-9370.0	940.0
1180	G120	-9390.0	815.0
1191	G98	-9610.0	940.0
1192	G96	-9630.0	815.0
1193	G94	-9650.0	940.0
1194	G92	-9670.0	815.0
1195	G90	-9690.0	940.0
1196	G88	-9710.0	815.0
1197	G86	-9730.0	940.0
1198	G84	-9750.0	815.0
1199	G82	-9770.0	940.0
1200	G80	-9790.0	815.0
1201	G78	-9810.0	940.0
1202	DMY12	-9830.0	815.0
1203	DMY13	-9850.0	940.0
1204	DMY14	-10135.0	960.0
1205	DMY15	-10115.0	575.0
1206	DMY16	-9990.0	545.0
1207	G76	-10115.0	515.0
1208	G74	-9990.0	485.0
1209	G72	-10115.0	455.0
1210	G70	-9990.0	425.0
1211	G68	-10115.0	395.0
1212	G66	-9990.0	365.0
1213	G64	-10115.0	335.0
1214	G62	-9990.0	305.0
1215	G60	-10115.0	275.0
1216	G58	-9990.0	245.0
1217	G56	-10115.0	215.0
1218	G54	-9990.0	185.0
1219	G52	-10115.0	155.0
1220	G50	-9990.0	125.0
1221	G48	-10115.0	95.0
1222	G46	-9990.0	65.0
1223	G44	-10115.0	35.0
1224	G42	-9990.0	5.0
1225	G40	-10115.0	-25.0
1226	G38	-9990.0	-55.0
1227	G36	-10115.0	-85.0
1228	G34	-9990.0	-115.0
1229	G32	-10115.0	-145.0
1230	G30	-9990.0	-175.0
1231	G28	-10115.0	-205.0
1232	G26	-9990.0	-235.0
1233	G24	-10115.0	-265.0
1234	G22	-9990.0	-295.0
1235	G20	-10115.0	-325.0

No.	Terminal name	X	Y
1236	G18	-9990.0	-355.0
1237	G16	-10115.0	-385.0
1238	G14	-9990.0	-415.0
1239	G12	-10115.0	-445.0
1240	G10	-9990.0	-475.0
1241	G8	-10115.0	-505.0
1242	G6	-9990.0	-535.0
1243	G4	-10115.0	-565.0
1244	G2	-9990.0	-595.0
1245	VGLDMY4	-10115.0	-625.0

Alignment mark	X	Y
+	10020.0	915.0
	-10020.0	915.0

Revision History

Revision	Date	Contents
0.00	2005.07.28	First release
0.01	2005.09.16	• Add the item of “Functions of bloks”. • Add the item of “GRAM address map”. • Add the item of “Instructions”. • Add the item of “System Interfaces”. • Add the item of “Instruction setup flow”. • Add the item of “Pattern Diagram for Voltage Setting”. • Add the item of “External Element Specifications”. • Add the item of “Absolute Maximum Ratings”. • Add the item of “Electrical characteristics [Target specifications are T.B.D]”.
0.02	2005.10.28	• Add the item of “RAM Address and Display Position on Panel” • Add the item of “Resize Function” • Add the item of “High-Speed RAM Write Mode” • Add the item of “Window Address Function” • Add the item of “Oscllagor” • Add the item of “n-Line Inversion Liquid Crystsl Drive” • Add the item of “Frame Frequency Adjustment Function” • Add the item of “γ-Control Circuit” • Add the item of “8-Color Display Mode” • Add the item of “Partisl Display Function”
0.03	2005.12.26	• Releas electrical characteristics. • Errors corrected.