eKTF5705

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.7

ELAN MICROELECTRONICS CORP.
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APPENDIX

Specification Revision History

Version	Revision Description	Date
1.0	Initial Release Version	2011/04/09
1.1	1. Added eKTF5705 2. Added wake-up time information 3. Modified the PWM start description 4. Deleted the eKTF5701QN24A Package type 5. Added note description in the "Instruction Set Table" 6. Modified the Pin assignment and description for VREC pin	2011/06/17
1.2	Modified the Port8 pull-high, open-drained and high drive/sink description	2011/07/12
1.3	1. Modified the code option description. 2. Modified Section 6.2 *TCC/WDT and Prescaler* description 3. Deleted register Bank1 R4A~R4C	2011/10/28
1.4	1. Added pin assignment for eKTF5701SO24 package type 2. Modified the entries in the DC Electrical Characteristics table.	2012/01/17
1.5	Deleted all information related to eKTF5701 spec.	2012/08/30
1.6	Modified the General Description section.	2012/10/11
1.7	1. Added TP Register & description 2. Modified the package information	2016/03/23

1 General Description

The eKTF5705 is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. It has a built-in 8K×15-bit programmable ROM and is equipped with touch sensors. The capacitive touchpad sensor uses plastic or glass substrate as cover.

The system controller converts fingertip position data into button presses, depending on finger location and human interface context. The ELAN eKTR5700 can be used to develop user program for this microcontroller and several other ELAN Flash type ICs.

2 Features

- CPU Configuration
  - 8K×15 bits on-chip ROM
  - 1072 (8 bits on-chip registers (SRAM)
  - 8-level stacks for subroutine nesting
  - Typically 5 μA during Sleep mode
  - 2 programmable Level Voltage Reset LVR : 3.0, 2.7V
  - Four CPU operating modes: Normal, Sleep, Green and Idle
- I/O Port Configuration
  - Four bidirectional I/O ports
  - 18 I/O pins
  - Four programmable pin change wake-up ports: P5, P6, P7, P8
  - Four programmable pull-down I/O ports: P5~P8
  - Four programmable open-drain I/O ports: P5~P8
  - Four programmable high-sink/drive I/O ports: P5, P6, P7, P8
- Operating Voltage Range:
  - 2.5V~3.6V at -40~85°C (Industrial)
- Operating Frequency Range (base on 2 clocks):
  - Main Oscillator:
    IRC mode: DC~16MHz @ 2.5V

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.5~3.6V)	Process	Total
4 MHz	± 2%	± 1%	± 1%	± 4%
8 MHz	± 2%	± 1%	± 1%	± 4%
12 MHz	± 2%	± 1%	± 1%	± 4%
16 MHz	± 2%	± 1%	± 1%	± 4%

  - Sub Oscillator:
    IRC mode: 16k/64k
- Peripheral Configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources (Fm/Fs)
  - 2-channel Digital-to-Analog Converter for 256 steps
  - Two 16-bit timers (TMR1/TMR2) with PWM function
  - Serial transmitter/receiver interface (SPI): 3-wire synchronous communication
  - I^2C function with 7/10-bit address and 8-bit data transmit/receive mode
  - Power down (Sleep) mode
  - High EFT immunity (4KV)
- 11 Available Interrupts:
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake-up from Sleep mode)
  - External interrupt
  - Two Timer interrupts
  - I^2C transfer/receive interrupt
  - SPI interrupt
- Single Instruction Cycle Commands
- Package Type:
  - 24 QFN 4×4×0.8mm : eKTF5705QN24
  - 24 SOP 300 mil : eKTF5705SO24

Note: *These are all Green products which do not contain hazardous substances.*

3 Pin Assignment

3.1 Package: QFN 24

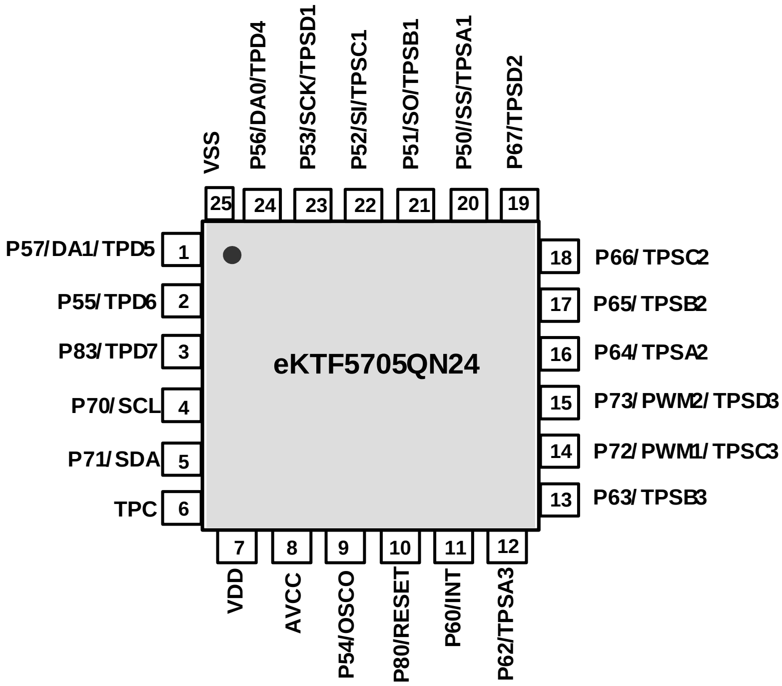


Figure 3-1 QFN-24 Pin Assignment

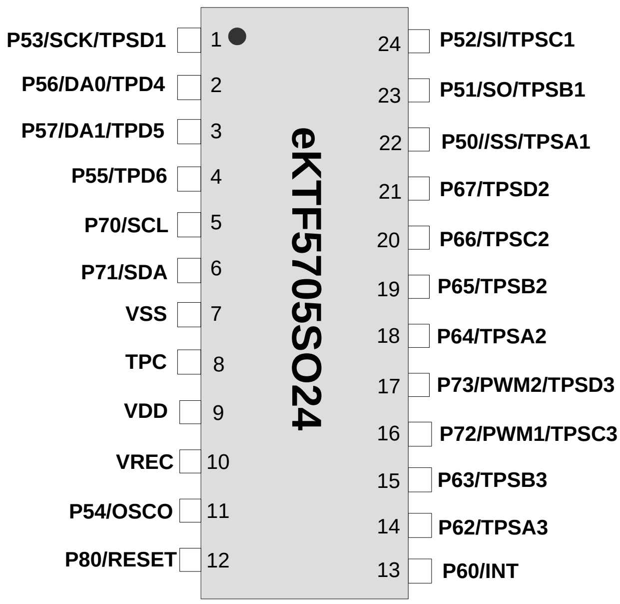


Figure 3-2 SOP-24 Pin Assignment

4 Pin Description

4.1 eKTF5705 Kernel Pin

Name	Function	Input Type	Output Type	Description
P50 / /SS / TPSA1	P50	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software. They can also be set to open-drain and enable high sink/drive modes by software.
	/SS	ST	-	SPI Slave mode enable (/SS)
	TPSA1	AN	AN	Touchpad sensor pins
P51 / SO / TPSB1	P51	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	SO	-	CMOS	SPI Serial Data Output (SO)
	TPSB1	AN	AN	Touchpad sensor pins
P52 / SI / TPSC1	P52	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	SI	ST	-	SPI Serial Data Input (SI)
	TPSC1	AN	AN	Touchpad sensor pins
P53 / SCK / TPSD1	P53	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	SCK	ST	CMOS	SPI Serial Clock Input/Output (SCK).
	TPSD1	AN	AN	Touchpad sensor pins
P54 / OSCO	P54	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	OSCO	-	CMOS	Clock output of internal RC oscillaor.
P55 / TPD6	P55	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	TPD6	-	AN CMOS	Touchpad driver pin.

(Continuation)

Name	Function	Input Type	Output Type	Description
P56 / DA0 / TPD4	P56	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	DA0	-	AN	Digital-to-Analog Converter (DAC)
	TPD4	-	AN CMOS	Touchpad driver pin.
P57 / DA1 / TPD5	P57	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	DA1	-	AN	Digital-to-Analog Converter (DAC)
	TPD5	-	AN CMOS	Touchpad driver pin.
P60 / INT	P60	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	INT	ST	-	External interrupt pin triggered by falling or rising edge (set by EIESCR).
P62 / TPSA3	P62	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	TPSA3	AN	AN	Touchpad sensor pins
P63 / TPSB3	P63	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	TPSB3	AN	AN	Touchpad sensor pins
P64 / TPSA2	P64	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	TPSA2	AN	AN	Touchpad sensor pins

(Continuation)

Name	Function	Input Type	Output Type	Description
P65 / TPSB2	P65	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	TPSB2	AN	AN	Touchpad sensor pins
P66 / TPSC2	P66	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	TPSC2	AN	AN	Touchpad sensor pins
P67 / TPSD2	P67	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	TPSD2	AN	AN	Touchpad sensor pins
P70 / SCL	P70	ST	CMOS	Bidirectional I/O ports. All can be pulled-down and pulled-high internally by software control. They also can be open-drain and enable high sink/drive mode by software control.
	SCL	ST	CMOS	I^2C Serial Clock Input/Output (SCL) [1]
P71 / SDA	P71	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	SDA	ST	CMOS	I^2C Serial Data Input/Output (SDA) [2]
P72 / PWM1 / TPSC3	P72	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	PWM1	-	CMOS	Pulse Width Modulation 1 outputs
	TPSC3	AN	AN	Touchpad sensor pins

[1] *Slave Address 0x77 is reserved for WTR use.*
[2] *Slave Address 0x77 is reserved for WTR use.*

(Continuation)

Name	Function	Input Type	Output Type	Description
P72 / PWM1 / TPSC3	P72	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	PWM1	-	CMOS	Pulse Width Modulation 1 output
	TPSC3	AN	AN	Touchpad sensor pins
P73 / PWM2 / TPSD3	P73	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	PWM2	-	CMOS	Pulse Width Modulation 2 outputs.
	TPSD3	AN	AN	Touchpad sensor pins
P80 / RESET	P80	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	RESET	ST	-	Schmitt trigger input pin. If this pin remains at logic low, the controller is reset. Internal pull-high reset pin.
P83 / TPD7	P83	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open-drain and enable high sink/drive modes by software.
	TPD7	-	AN CMOS	Touchpad driver pin
VDD	VDD	Power	-	Power supply pin
VSS	VSS	Power	-	Ground
TPC	TPC	AN	-	Touchpad capacitor [3]
VREC	VREC	AN	-	Voltage reference external capacitor [4]

[3] *TPC external capacitor is 1 μf, stable time is 300 μs.*
[4] *VREC external capacitor is 2 μf.*

4.2 Compound Pin Function Priority

- Priority of Pin P50/SS/TPSA1:

Pin Priority		
1st	2nd	3rd
TPSA1	/SS	P50

- Priority of Pin P51/SO/TPSB1:

Pin Priority		
1st	2nd	3rd
TPSB1	SO	P51

- Priority of Pin P52/SI/TPSC1:

Pin Priority		
1st	2nd	3rd
TPSC1	SI	P52

- Priority of Pin P53/SCK/TPSD1:

Pin Priority		
1st	2nd	3rd
TPSD1	SCK	P53

- Priority of Pin P54/OSCO:

Pin Priority	
1st	2nd
OSCO	P54

- Priority of Pin P55/TPD6:

Pin Priority	
1st	2nd
TPD6	P55

- Priority of Pin P56/DA0/TPD4:

Pin Priority	
1st	2nd
TPD4 & DA0	P56

- Priority of Pin P57/DA1/TPD5**:**

Pin Priority	
1^{st}	2^{nd}
TPD5 and DA1	P57

- Priority of Pin P60/INT**:**

Pin Priority	
1^{st}	2^{nd}
INT	P60

- Priority of Pin P62/TPSA3**:**

Pin Priority	
1^{st}	2^{nd}
TPSA3	P62

- Priority of Pin P63/TPSB3:

Pin Priority	
1^{st}	2^{nd}
TPSB3	P63

- Priority of Pin P64/TPSA2:

Pin Priority	
1^{st}	2^{nd}
TPSA2	P64

- Priority of Pin P65/TPSB2:

Pin Priority	
1^{st}	2^{nd}
TPSB2	P65

- Priority of Pin P66/TPSC2:

Pin Priority	
1^{st}	2^{nd}
TPSC2	P66

- Priority of Pin P67/TPSD2:

Pin Priority	
1st	2nd
TPSD2	P67

- Priority of Pin P72/PWM1/TPSC3:

Pin Priority		
1st	2nd	3rd
TPSC3	PWM1	P72

- Priority of Pin P73/PWM2/TPSD3:

Pin Priority		
1st	2nd	3rd
TPSD3	PWM2	P73

- Priority of Pin P83/TPD7:

Pin Priority	
1st	2nd
TPD7	P83

5 Functional Block Diagram

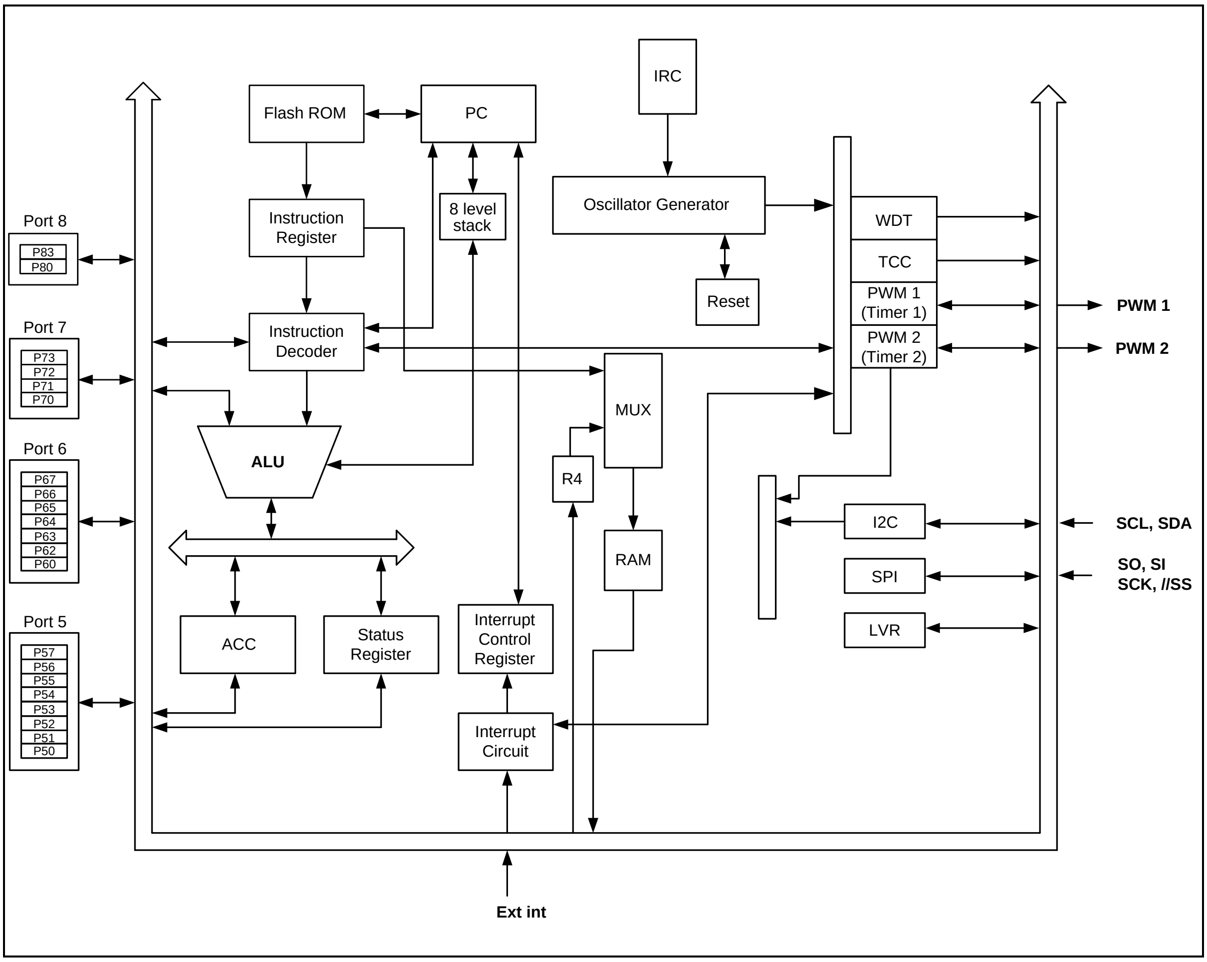


Figure 5-1 eKTF5705 Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0: IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1: BSR (Bank Selection Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	SBS1	SBS0	-	GBS2	GBS1	GBS0
-	-	R/W	R/W	0	R/W	R/W	R/W

Bits 7~6: Not used. Set to "0" all the time.

Bits 5~4 (SBS1~SBS0): Special register bank select bit. It is used to select Banks 0/1/2 of Special Registers **R5~R4F**.

SBS1	SBS0	Special Register Bank
0	**0**	0
0	**1**	1
1	**0**	2
1	**1**	X

Bit 3: Not used. Set to "0" all the time.

Bits 2~0 (GBS2~GBS0): General register bank select bit. It is used to select Banks 0~7 of General Registers **R80~RFF**.

GBS2	GBS1	GBS0	RAM Bank
0	**0**	**0**	0
0	**0**	**1**	1
0	**1**	**0**	2
0	**1**	**1**	3
1	**0**	**0**	4
1	**0**	**1**	5
1	**1**	**0**	6
1	**1**	**1**	7

6.1.3 R2: PCL (Program Counter Low)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PC7~PC0): The low byte of program counter.

- Depending on the device type, R2 and hardware stack are 15-bit wide. The structure is depicted in Figure 6-1 below.
- Generates 8K×15 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 4096 words long.
- R2 is set as all "**0**"s when under RESET condition.
- "JMP" instruction allows direct loading of the lower 12 program counter bits. Thus, "JMP" allows PC to go to any location within a page.
- "CALL" instruction loads the lower 12 bits of the PC, and the present PC value will add **1** and is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the lower 13 program counter bits. Therefore, "LJMP" allows PC to jump to any location within 8K (2^{13}).
- "LCALL" instruction loads the lower 13 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within 8K (2^{13}).
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC won’t be changed.
- Any instruction, except “ADD R2,A” that is written to R2 (e.g., "MOV R2, A", "BC R2, 6",”INC R2”, etc.) will cause the ninth bit and the above bits (A8~A12) of the PC to remain unchanged.
- All instructions are single instruction cycle (Fsys/2) except “LCALL”, ”CALL”, ”LJMP”, and “JMP” instructions. The “LCALL” and “LJMP” instructions need two instructions cycle.

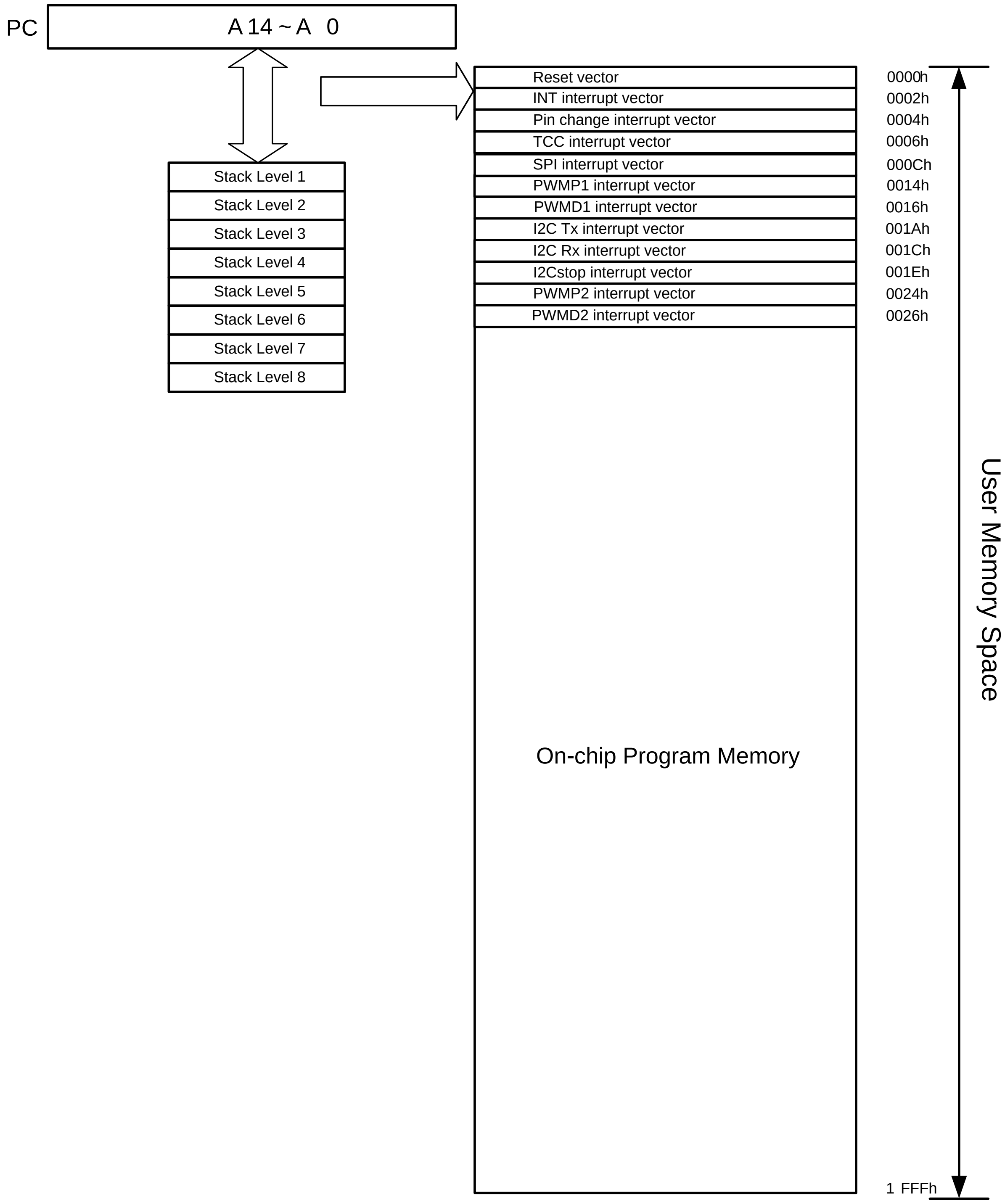


Figure 6-1 eKTF5705 Program Counter Organization

Data Memory Configuration

Address	Bank 0	Bank 1	Bank 2
0X00	IAR (Indirect Addressing Register)		
0X01	BSR (Bank Selection Control Register)		
0X02	PCL (Program Counter Low)		
0X03	SR (Status Register)		
0X04	RSR (RAM Selection Register)		
0X05	Port 5	IOCR8	Unused
0X06	Port 6	Unused	Unused
0X07	Port 7	Unused	Unused
0X08	Port 8	P5PHCR	Unused
0X09	Unused	P6PHCR	Unused
0X0A	Unused	P78PHCR	Unused
0x0B	IOCR5	P5PLCR	Unused
0X0C	IOCR6	P6PLCR	Unused
0X0D	IOCR7	P78PLCR	Unused
0X0E	OMCR (Operating Mode Control Register)	P5HDSCR	Unused
0X0F	EIESCR (External Interrupt Edge Select Control Register)	P6HDSCR	Unused
0X10	WUCR1	P78HDSCR	Unused
0X11	WUCR2	P5ODCR	Unused
0X12	WUCR3	P6ODCR	Unused
0X13	Unused	P78ODCR	Unused
0X14	SFR1 (Status Flag Register 1)	Unused	Unused
0X15	Unused	Unused	Unused
0X16	SFR3 (Status Flag Register 3)	PWMSCR	Unused
0X17	SFR4 (Status Flag Register 4)	PWM1CR	Unused
0X18	Unused	PRD1L	Unused
0X19	Unused	PRD1H	Unused
0X1A	Unused	DT1L	Unused
0X1B	IMR1 (Interrupt Mask Register 1)	DT1H	Unused
0X1C	Unused	TMR1L	Unused
0X1D	IMR3 (Interrupt Mask Register 3)	TMR1H	Unused
0X1E	IMR4 (Interrupt Mask Register 4)	PWM2CR	Unused
0X1F	Unused	PRD2L	Unused
0X20	Unused	PRD2H	Unused
0X21	WDTCR	DT2L	DACR

(Continuation)

Address	Bank 0	Bank 1	Bank 2
0X22	TCCCR	DT2H	DACD0
0X23	TCCD	TMR2L	DACD1
0X24	Unused	TMR2H	Unused
0X25	Unused	Unused	Unused
0X26	Unused	Unused	Unused
0X27	Unused	Unused	Unused
0X28	Unused	Unused	Unused
0X29	Unused	Unused	Unused
0X2A	Unused	Unused	Unused
0x2B	Unused	Unused	Unused
0X2C	Unused	Unused	Unused
0X2D	Unused	Unused	Unused
0X2E	Unused	Unused	Unused
0X2F	Unused	Unused	Unused
0X30	I2CCR1	Unused	Unused
0X31	I2CCR2	Unused	Unused
0X32	I2CSA	Unused	Unused
0X33	I2CDB	Unused	Unused
0X34	I2CDAL	Unused	Unused
0X35	I2CDAH	Unused	Unused
0X36	SPICR	Unused	Unused
0X37	SPIS	Unused	Unused
0X38	SPIR	Unused	Unused
0X39	SPIW	Unused	Unused
0X3A	Unused	Unused	Unused
0x3B	Unused	Unused	Unused
0X3C	Unused	Unused	Unused
0X3D	Unused	Unused	Unused
0X3E	Unused	Unused	Unused
0X3F	Unused	Unused	Unused
0X40	Unused	Unused	Unused
0X41	Unused	Unused	Unused
0X42	Unused	Unused	Unused
0X43	Unused	Unused	Unused
0X44	Unused	Unused	Unused
0X45	Unused	TBPTL	Unused

(Continuation)

0X46	Unused	TBPTH	Unused
0X47	Unused	STKMON	Unused
0X48	Unused	PCH	Unused
0X49	Unused	Unused	Unused
0X4A	Unused	Unused	Unused
0x4B	Unused	Unused	Unused
0X4C	Unused	Unused	Unused
0X4D	Unused	Unused	Unused
0X4E	Unused	Unused	Unused
0X4F	Unused	Unused	Unused
0X50 0X51 : : 0X7F	General Purpose Register		

0X80 0X81 : : : 0XFE 0XFF	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7

6.1.4 R3: SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT	-	-	T	P	Z	DC	C
F	-	-	R/W	R/W	R/W	R/W	R/W

Bit 7 (INT): Interrupt Enable flag

0: Interrupt masked by DISI or hardware interrupt

1: Interrupt enabled by ENI/RETI instructions

> **NOTE**
> *INT bit cannot be saved by hardware when interrupt occurs.*

Bits 6~5: Not used. Set to "**0**" all the time.

Bit 4 (T): Time-out bit

Set to “**1**” with the "SLEP" and "WDTC" commands, or during power up.

Reset to “**0**” by WDT time-out.

Bit 3 (P): Power down bit.

Set to “1” during power on or by a "WDTC" command.

Reset to “0” by a "SLEP" command.

Bit 2 (Z): Zero flag.

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4: RSR (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (RSR7~RSR0): These bits are used to select registers (Address 00 ~ FF) in indirect addressing mode. For more details, refer to the table on Data Memory Configuration in Section 6.1.3, *R2: PCL (Program Counter Low)*.

6.1.6 Bank 0 R5 ~ R8: (Port 5 ~ Port 8)

R5, R6, R7, and R8 are I/O data registers.

6.1.7 Bank 0 R9 ~ RA: (Reserved)

6.1.8 Bank 0 RB~RD: (IOCR5 ~ IOCR7)

These registers are used to control I/O port direction. They are both readable and writable.

0: Set the relative I/O pin as output

1: Set the relative I/O pin into high impedance

6.1.9 Bank 0 RE: OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	-	-	-	-	RCM1	RCM0
R/W	R/W	-	-	-	-	R/W	R/W

Bit 7 (CPUS): CPU Oscillator Source Select

0: Fs**:** sub-oscillator

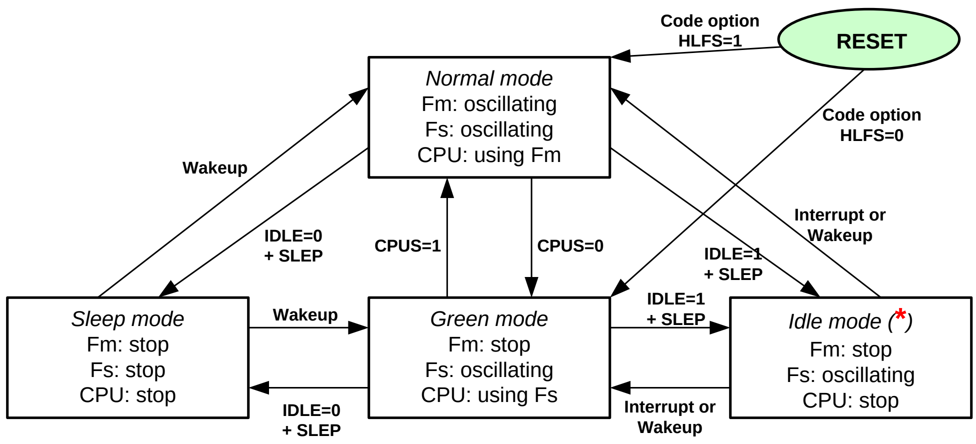
1: Fm**:** main-oscillator (default)

When CPUS = **0**, the CPU oscillator selects the sub-oscillator while the main oscillator is stopped.

Bit 6 (IDLE): Idle Mode Enable Bit. This bit decides which mode (see figure below) to use with the SLEP instruction.

0: "IDLE = **0**" + SLEP instruction → Sleep mode

1: "IDLE = **1**" + SLEP instruction → Idle mode (default)



*<u>Switching operation mode at Idle → Normal, Idle → Green:</u>

*If the clock source of timer is **Fs**, the timer/counter will continue to count during Idle mode. When a match condition of the timer/counter occurs during Idle mode, the interrupt flag of timer/counter is activated. However, the MCU will jump to interrupt vector when the corresponding interrupt is enabled.*

Figure 6-2 CPU Operation Mode

■ Oscillation Characteristics

CPU Mode Switch	Waiting Time before CPU Resumes Working
Sleep → Normal	WSTO + 8/32 clocks (main frequency)
Idle → Normal	WSTO + 8/32 clocks (main frequency)
Green → Normal	WSTO + 8/32 clocks (main frequency)
Sleep → Green	WSTO + 8 clocks (sub frequency)
Idle → Green	WSTO + 8 clocks (sub frequency)
Normal → Normal	8 clocks (main frequency)
Green → Green	6~10 clocks (sub frequency)

***WSTO:** Waiting time for Start-to-Oscillation*

Bits 5~2: Not used. Set to "**0**" all the time.

Bits 1~0 (RCM1~RCM0): Internal RC mode selection bits

*RCM1	*RCM0	Frequency (MHz)
0	**0**	12
0	**1**	8
1	**0**	16
1	**1**	4

6.1.10 Bank 0 RF: EIESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EIES	-	-
-	-	-	-	-	R/W	-	-

Bits 7~3: Not used. Set to "**0**" all the time.

Bit 2 (EIES): External interrupt edge select bit

0: Falling edge interrupt

1: Rising edge interrupt

Bits 1~0: Not used. Set to "**0**" all the time.

6.1.11 Bank 0 R10: WUCR1 (Wake-up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	INTWK	-	-
-	-	-	-	-	R/W	-	-

Bits 7~3: Not used. Set to "**0**" all the time.

Bit 2 (INTWK): External Interrupt (INT pin) Wake-up Function Enable Bit

0: Disable External Interrupt wake-up

1: Enable External Interrupt wake-up

When the External Interrupt status change is used to enter interrupt vector or to wake-up IC from Sleep/Idle mode, the INTWK bits must be set to "Enable".

Bits 1~0: Not used. Set to "**0**" all the time.

6.1.12 Bank 0 R11: WUCR2 (Wake-up Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	SPIWK	I2CWK	-	-
-	-	-	-	RR/W	R/W	-	-

Bits 7~4: Not used. Set to "**0**" all the time.

Bit 3 (SPIWK): SPI wake-up enable bit. Applicable when SPI works in Slave mode.

0: Disable SPI wake-up

1: Enable SPI wake-up

Bit 2 (I2CWK): I^{2}C wake-up enable bit. Applicable when I^{2}C works in Slave mode.

0: Disable I^{2}C wake-up

1: Enable I^{2}C wake-up

> **NOTE**
> *When I^{2}C is in Slave mode, it cannot communicate with MCU in Green mode. At the same time the SCL in on hold and kept at low level when MCU is in Green mode. SCL is released when MCU switches to Normal mode.*

Bits 1~0: Not used. Set to "**0**" all the time.

6.1.13 Bank 0 R12: WUCR3 (Wake-up Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICWKP8	ICWKP7	ICWKP6	ICWKP5	-	-	-	-
R/W	R/W	R/W	R/W	-	-	-	-

Bits 7~4 (ICWKP8~ICWKP5): Pin change Wake-up enable for Ports 8/7/6/5.

0: Disable wake-up function

1: Enable wake-up function

Bits 3~0: Not used. Set to "**0**" all the time.

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
Pin Change INT	ICWKPx = 0, PxICIE = 0	Wake-up is invalid				Interrupt is invalid			
	ICWKPx = 0, PxICIE = 1	Wake-up is invalid				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWKPx = 1, PxICIE = 0	Wake-up + Next Instruction				Interrupt is invalid			
	ICWKPx = 1, PxICIE = 1	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

> **NOTE**
> *When the MCU wakes up from Sleep or Idle mode, the ICSF must be equal to **1**. If ICSF is equal to **0**, it means the pin status does not change or the pin change ICIE is disabled. Hence the MCU cannot wake-up.*

6.1.14 Bank 0 R13: (Reserved)

6.1.15 Bank 0 R14: SFR1 (Status Flag Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXSF	-	TCSF
-	-	-	-	-	F	-	F

Each corresponding status flag is set to "**1**" when interrupt condition is triggered.

Bits 7~3, 1: Not used. Set to "**0**" all the time.

Bit 2 (EXSF): External interrupt status flag

Bit 0 (TCSF): TCC overflow status flag. Set when TCC overflows. Reset by software.

> **NOTE**
> *If a function is enabled, the corresponding status flag would be active regardless of whether the interrupt mask is enabled or not.*

6.1.16 Bank 0 R15: (Reserved)

6.1.17 Bank 0 R16: SFR3 (Status Flag Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	PWM2PSF	PWM2DSF	PWM1PSF	PWM1DSF
-	-	-	-	F	F	F	F

Bits 7~4: Not used. Set to "**0**" all the time.

Bit 3 (PWM2PSF): Status flag of period-matching for PWM2 (Pulse Width Modulation). Set when a selected period is reached. Reset by software.

Bit 2 (PWM2DSF): Status flag of duty-matching for PWM2 (Pulse Width Modulation). Set when a selected duty is reached. Reset by software.

Bit 1 (PWM1PSF): Status flag of period-matching for PWM1 (Pulse Width Modulation). Set when a selected period is reached. Reset by software.

Bit 0 (PWM1DSF): Status flag of duty-matching for PWM1 (Pulse Width Modulation). Set when a selected duty is reached. Reset by software.

> **NOTE**
> *If a function is enabled, the corresponding status flag would be active whether the interrupt mask is enabled or not.*

6.1.18 Bank 0 R17: SFR4 (Status Flag Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8ICSF	P7ICSF	P6ICSF	P5ICSF	SPISF	I2CSTPSF	I2CRSF	I2CTSF
F	F	F	F	F	F	F	F

Bits 7~4 (P8ICSF~P5ICSF): Ports 5~8 input status change status flag. Set when Ports 5~8 input changes. Reset by software.

Bit 3 (SPISF): SPI mode status flag. Flag is cleared by software.

Bit 2 (I2CSTPSF): I^2C stop status flag. Set when I^2C stop signal occurs.

Bit 1 (I2CRSF): I^2C receive status flag. Set when I^2C receives 1byte data and responds ACK signal. Reset by firmware or I^2C disable.

Bit 0 (I2CTSF): I^2C transmit status flag. Set when I^2C transmits 1 byte data and receive handshake signal (ACK or NACK). Reset by firmware or I^2C disable

NOTE

If a function is enabled, the corresponding status flag will be active regardless whether the interrupt mask is enabled or not.

6.1.19 Bank 0 R18~R1A: (Reserved)

6.1.20 Bank 0 R1B: IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIE	-	TCIE
-	-	-	-	-	R/W	-	R/W

Bits 7~3, 1: Not used. Set to "**0**" all the time.

Bit 2 (EXIE): EXSF interrupt enable and **/INT** function enable bit

0: P60/INT is P60 pin. EXSF is always equal **0**.

1: Enable EXSF interrupt and P60/INT is /INT pin

Bit 0 (TCIE): TCSF interrupt enable bit.

0: Disable TCSF interrupt

1: Enable TCSF interrupt

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter will jump into corresponding interrupt vector when the corresponding status flag is set.

6.1.21 Bank 0 R1C: (Reserved)

6.1.22 Bank 0 R1D: IMR3 (Interrupt Mask Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	PWM2PIE	PWM2DIE	PWM1PIE	PWM1DIE
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7~4: Not used. Set to "**0**" all the time.

Bit 3 (PWM2PIE): PWM2PSF interrupt enable bit
0: Disable period-matching of PWM2 interrupt
1: Enable period-matching of PWM2 interrupt

Bit 2 (PWM2DIE): PWM2DSF interrupt enable bit
0: Disable duty-matching of PWM2 interrupt
1: Enable duty-matching of PWM2 interrupt

Bit 1 (PWM1PIE): PWM1PSF interrupt enable bit
0: Disable period-matching of PWM1 interrupt
1: Enable period-matching of PWM1 interrupt

Bit 0 (PWM1DIE): PWM1DSF interrupt enable bit
0: Disable duty-matching of PWM1 interrupt
1: Enable duty-matching of PWM1 interrupt

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter will jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.23 Bank 0 R1E: IMR4 (Interrupt Mask Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8ICIE	P7ICIE	P6ICIE	P5ICIE	SPIIE	I2CSTPIE	I2CRIE	I2CTIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~4 (P8ICIE~P5ICIE): PxICSF interrupt enable bit
0: Disable PxICSF interrupt
1: Enable PxICSF interrupt

Bit 3 (SPIIE): Interrupt enable bit
0: Disable SPSF interrupt
1: Enable SPSF interrupt

Bit 2 (I2CSTPIE): I^2C stop interrupt enable bit.
0: Disable interrupt
1: Enable interrupt

Bit 1 (I2CRIE): I^2C Interface Rx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

Bit 0 (I2CTIE): I^2C Interface Tx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

> **NOTE**
> *If the interrupt mask and instruction "ENI" are enabled, the program counter will jump into the corresponding interrupt vector when the corresponding status flag is set.*

6.1.24 Bank 0 R1F~R20: (Reserved)

6.1.25 Bank 0 R21: WDTCR (Watchdog Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	-	-	-	PSWE	WPSR2	WPSR1	WPSR0
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (WDTE): Watchdog Timer enable bit. WDTE is both readable and writable.

0: Disable WDT

1: Enable WDT

Bits 6~4: Not used. Set to "**0**" all the time.

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disable bit. WDT rate is 1:1.

1: Prescaler enable bit. WDT rate is set at bits 2~0.

Bits 2~0 (WPSR2~WPSR0): WDT Prescaler bits

WPSR2	WPSR1	WPSR0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.26 Bank 0 R22: TCCCR (TCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TCCS	-	-	PSTE	TPSR2	TPSR1	TPSR0
0	R/W	0	0	R/W	R/W	R/W	R/W

Bit 7: Not used. Set to "**0**" all the time.

Bit 6 (TCCS): TCC Clock Source select bit

0: Fs (sub clock)

1: Fm (main clock)

Bits 5~4: Not used. Set to "**0**" all the time.

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disable bit. TCC rate is 1:1.

1: Prescaler enable bit. TCC rate is set at Bit 2 ~ Bit 0.

Bits 2~0 (TPSR2~TPSR0): TCC Prescaler Bits

TPSR2	TPSR1	TPSR0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.27 Bank 0 R23: TCCD (TCC Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TCC7~TCC0): TCC data

Counter is increased by the instruction cycle clock. Writable and readable as any other registers.

6.1.28 Bank 0 R24 ~ R2F: (Reserved)

6.1.29 Bank 0 R30: I2CCR1 (I^2C Status and Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY
R/W	R/W	R/W	R/W	R	R	R	R

Bit 7 (Strobe/Pend): In Master mode, it is used as strobe signal to control I^2C circuit in sending SCL clock. Automatically resets after receiving or transmitting handshake signal (ACK or NACK). In Slave mode, it is used as pending signal. User should clear it after writing data into Tx buffer or taking data from Rx buffer to inform Slave I^2C circuit to release SCL signal.

Bit 6 (IMS): I^2C Master/Slave mode select bit

0: Slave (Default)

1: Master

Bit 5 (ISS): I^2C C Fast/Standard mode select bit (if Fm is 4MHz and I2CTS1~0<0,0>)

0: Standard mode (100K bit/s)

1: Fast mode (400K bit/s)

Bit 4 (STOP): In Master mode, if STOP=1 and R/nW=1, then MCU must return nACK signal to Slave device before sending STOP signal. If STOP=1 and R/nW=0, then MCU sends STOP signal after receiving an ACK signal. MCU resets when it sends STOP signal to Slave device.

In Slave mode, if STOP=1 and R/nW=0 then MCU must return nACK signal to Master device.

Bit 3 (SAR_EMPTY): Set when MCU transmits 1 byte data from I^2C Slave Address Register and receive ACK (or nACK) signal. Reset when MCU writes 1 byte data to I^2C Slave Address Register.

Bit 2 (ACK): The ACK condition bit is set to 1 by hardware when the device responds acknowledge (ACK). Resets when the device responds with a not-acknowledge (nACK) signal

Bit 1 (FULL): Set by hardware when I^2C Receive Buffer register is full. Reset by hardware when MCU reads data from I^2C Receive Buffer register.

Bit 0 (EMPTY): Set by hardware when I^2C Transmit Buffer register is empty and ACK (or nACK) signal is received. Reset by hardware when MCU writes new data into I^2C Transmit Buffer register.

6.1.30 Bank 0 R31: I2CCR2 (I^2C Status and Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CBF	GCEN	-	BBF	I2CTS1	I2CTS0	-	I2CEN
R	R/W	-	R	R/W	R/W	-	R/W

Bit 7 (I2CBF): I^2C Busy Flag Bit

0: Clear to "**0**" under Slave mode if the received STOP signal or I^2C Slave Address does not match

1: Set when I^2C communicate with Master in Slave mode

> **NOTE**
> *Set when START signal occurs. Clear when I^2C is disabled or STOP signal ocurs for Slave mode.*

Bit 6 (GCEN): I^2C General Call Function Enable bit

0: Disable General Call Function

1: Enable General Call Function

Bit 5: Not used. Set to "**0**" all the time.

Bit 4 (BBF): Busy Flag Bit. I^2C detection is busy in Master mode. Read only.

> **NOTE**
> *Set when START signal occurs. Clear when STOP signal ocurs for Master mode.*

Bits 3~2 (I2CTS1~I2CTS0): I^2C Transmit Clock select bits. When using different operating frequency (Fm), these bits must be set correctly in order for the SCL clock to be consistent with the Standard/Fast mode.

- I2CCR1 Bit5 = 1, Fast mode**:**

I2CTS1	I2CTS0	SCL CLK	Operating Fm (MHz)
0	**0**	Fm/10	4
0	**1**	Fm/20	8
1	**0**	Fm/30	12
1	**1**	Fm/40	16

- I2CCR1 Bit5 = 0, Standard mode**:**

I2CTS1	I2CTS0	SCL CLK	Operating Fm (MHz)
0	**0**	Fm/40	4
0	**1**	Fm/80	8
1	**0**	Fm/120	12
1	**1**	Fm/160	16

Bit 1: No used. Set to "**0**" all the time.

Bit 0 (I2CEN): I^2C Enable bit
0: Disable I^2C mode
1: Enable I^2C mode (default)

6.1.31 Bank 0 R32: I2CSA (I^2C Slave Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~1 (SA6~SA0): When the MCU is used as Master device for I^2C application, these bits are the Slave Device Address register.

Bit 0 (IRW): When the MCU is used as Master device for I^2C application, this bit is Read/Write transaction control bit.
0: Write
1: Read

6.1.32 Bank 0 R33: I2CDB (I^2C Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DB7~DB0): I^2C Receive/Transmit Data Buffer

6.1.33 Bank 0 R34: I2CDAL (I^2C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DA7~DA0): When the MCU is used as Slave device for I^2C application, this register stores the MCU address. It is used to identify the data on the I^2C bus to extract the message delivered to the MCU.

> **NOTE**
> *Slave Address 0x77 is reserved for WTR use.*

6.1.34 Bank 0 R35: I2CDAH (I^2C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	DA9	DA8
-	-	-	-	-	-	R/W	R/W

Bits 7~2: Not used. Set to "**0**" all the time.

Bits 1~0 (DA9~DA8): Device Address bits

6.1.35 Bank 0 R36: SPICR (SPI Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (CES): Clock Edge Select bit

0: Data shift-out on rising edge, and shift-in on a falling edge. Data is on hold during a low-level.

1: Data shift-out on falling edge, and shift-in on a rising edge. Data is on hold during a high-level.

Bit 6 (SPIE): SPI Enable bit

0: Disable SPI mode

1: Enable SPI mode

Bit 5 (SRO): SPI Read Overflow bit

0: No overflow

1: A new data is received while the previous data is still being held in the SPIR register. Under this condition, the data in SPIS register is destroyed. To avoid setting this bit, you should read the SPIR register although only the transmission is implemented. This can only occur in Slave mode.

Bit 4 (SSE): SPI Shift Enable bit

0: Reset as soon as the shift is completed, and the next byte is read to shift.

1: Start to shift, and remain at "**1**" while the current byte is still being transmitted.

Bit 3 (SDOC): SDO Output Status Control bit

0: After serial data output, the SDO remains high

1: After serial data output, the SDO remains low

Bits 2~0 (SBRS2~SBRS0): SPI Baud Rate Select bits

SBRS2	SBRS1	SBRS0	Mode	SPI Baud Rate
0	**0**	**0**	Master	Fosc/2
0	**0**	**1**	Master	Fosc/4
0	**1**	**0**	Master	Fosc/8
0	**1**	**1**	Master	Fosc/16
1	**0**	**0**	Master	Fosc/32
1	**0**	**1**	Master	Fosc/64
1	**1**	**0**	Slave	/SS enable
1	**1**	**1**	Slave	/SS disable

6.1.36 Bank 0 R37: SPIS (SPI Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DORD	TD1	TD0	0	OD3	OD4	0	RBF
R/W	R/W	R/W	-	R/W	R/W	-	R

Bit 7 (DORD): Data shift type control bit

0: Shift left (MSB first)

1: Shift right (LSB first)

Bits 6~5 (TD1~TD0): SDO status output delay time options (Normal mode only). When the CPU oscillator source uses Fs, it will result to 1 CLK delay time

NOTE

TD1~TD0 bits are applicable only to Normal mode → Normal mode. If under Sleep mode → Normal mode condition, then Wake-up time is "Warm up time + 1CLK".

TD1	TD0	Delay Time
0	**0**	8 CLK
0	**1**	16 CLK
1	**0**	24 CLK
1	**1**	32 CLK

Bit 4: Not used. Set to "**0**" all the time.

Bit 3 (OD3): Open-drain control bit

0: Open-drain disable for SDO

1: Open-drain enable for SDO

Bit 2 (OD4): Open-drain control bit

0: Open-drain disable for SCK

1: Open-drain enable for SCK

Bit 1: Not used. Set to "**0**" all the time.

Bit 0 (RBF): Read Buffer Full flag

0: Receiving not completed, and SPIR has not fully exchanged data.

1: Receiving completed, and SPIR has fully exchanged data.

6.1.37 Bank 0 R38: SPIR (SPI Read Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
R	R	R	R	R	R	R	R

Bits 7~0 (SRB7~SRB0): SPI Read Data Buffer

6.1.38 Bank 0 R39: SPIW (SPI Write Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (SWB7~SWB0): SPI Write Data Buffer

6.1.39 Bank 0 R3A ~ R4F: (Reserved)

6.1.40 Bank 1 R5: IOCR8

These registers are used to control I/O port direction. They are both readable and writable.

1: Put the relative I/O pin into high impedance

0: Put the relative I/O pin as output

6.1.41 Bank 1 R6 ~ R7: (Reserved)

6.1.42 Bank 1 R8: P5PHCR (Port 5 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH57	PH56	PH55	PH54	PH53	PH52	PH51	PH50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PH57): Control bit used to enable pull-high of the P57 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (PH56): Control bit used to enable pull-high of the P56 pin

Bit 5 (PH55): Control bit used to enable pull-high of the P55 pin

Bit 4 (PH54): Control bit used to enable pull-high of the P54 pin

Bit 3 (PH53): Control bit used to enable pull-high of the P53 pin

Bit 2 (PH52): Control bit used to enable pull-high of the P52 pin

Bit 1 (PH51): Control bit used to enable pull-high of the P51 pin

Bit 0 (PH50): Control bit used to enable pull-high of the P50 pin

6.1.43 Bank 1 R9: P6PHCR (Port 6 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	PH66	PH65	PH64	PH63	PH62	-	PH60
R/W	R/W	R/W	R/W	R/W	R/W	0	R/W

Bit 7 (PH67): Control bit used to enable pull-high of the P67 pin

Bit 6 (PH66): Control bit used to enable pull-high of the P66 pin

Bit 5 (PH65): Control bit used to enable pull-high of the P65 pin

Bit 4 (PH64): Control bit used to enable pull-high of the P64 pin

Bit 3 (PH63): Control bit used to enable pull-high of the P63 pin

Bit 2 (PH62): Control bit used to enable pull-high of the P62 pin

Bit 1: Not used. Set to "**0**" all the time.

Bit 0 (PH60): Control bit used to enable pull-high of the P60 pin

6.1.44 Bank 1 RA: P78PHCR (Ports 7~8 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	P8LPH	-	P7LPH
-	-	-	-	-	R/W	0	R/W

Bits 7~3, 1: Not used. Set to "**0**" all the time.

Bit 2 (P8LPH): Control bit used to enable pull-high of the Port 8 low nibble pin

Bit 0 (P7LPH): Control bit used to enable pull-high of the Port 7 low nibble pin

6.1.45 Bank 1 RB: P5PLCR (Port 5 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL57	PL56	PL55	PL54	PL53	PL52	PL51	PL50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PL57): Control bit used to enable pull-low of the P57 pin

0: Enable internal pull-low

1: Disable internal pull-low

Bit 6 (PL56): Control bit used to enable pull-low of the P56 pin

Bit 5 (PL55): Control bit used to enable pull-low of the P55 pin

Bit 4 (PL54): Control bit used to enable pull-low of the P54 pin

Bit 3 (PL53): Control bit used to enable pull low of the P53 pin

Bit 2 (PL52): Control bit used to enable pull-low of the P52 pin

Bit 1 (PL51): Control bit used to enable pull-low of the P51 pin

Bit 0 (PL50): Control bit used to enable pull-low of the P50 pin

6.1.46 Bank 1 RC: P6PLCR (Port 6 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL67	PL66	PL65	PL64	PL63	PL62	-	PL60
R/W	R/W	R/W	R/W	R/W	R/W	0	R/W

Bit 7 (PL67): Control bit used to enable pull-low of the P67 pin

Bit 6 (PL66): Control bit used to enable pull-low of the P66 pin

Bit 5 (PL65): Control bit used to enable pull-low of the P65 pin

Bit 4 (PL64): Control bit used to enable pull-low of the P64 pin

Bit 3 (PL63): Control bit used to enable pull-low of the P63 pin

Bit 2 (PL62): Control bit used to enable pull-low of the P62 pin

Bit 1: Not used. Set to "**0**" all the time.

Bit 0 (PL60): Control bit used to enable pull-low of the P60 pin

6.1.47 Bank 1 RD: P78PLCR (Ports 7~8 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	P8LPL	-	P7LPL
-	-	-	-	-	R/W	0	R/W

Bits 7~3, 1: Not used. Set to "**0**" all the time.

Bit 2 (P8LPH): Control bit used to enable pull-low of Port 8 low nibble pin

Bit 0 (P7LPH): Control bit used to enable pull-low of Port 7 low nibble pin

6.1.48 Bank 1 RE: P5HDSCR (Port 5 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H57	H56	H55	H54	H53	H52	H51	H50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (H57~H50): P57~P50 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.49 Bank 1 RF: P6HDSCR (Port 6 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H67	H66	H65	H64	H63	H62	-	H60
R/W	R/W	R/W	R/W	R/W	R/W	0	R/W

Bits 7~2, 0 (H67~H62,H60): P67~P62,P60 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

Bit 1: Not used. Set to "**0**" all the time.

6.1.50 Bank 1 R10: P78HDSCR (Port 7~8 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	P8LHDS	-	P7LHDS
-	-	-	-	-	R/W	0	R/W

Bits 7~3, 1: Not used. Set to "**0**" all the time.

Bit 2 (P8LHDS): Control bit used to enable high drive/sink of Port 8 low nibble pin

Bit 0 (P7LHDS): Control bit used to enable high drive/sink of Port 7 low nibble pin

6.1.51 Bank 1 R11: P5ODCR (Port 5 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (OD57~OD50): Open-Drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.52 Bank 1 R12: P6ODCR (Port 6 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	-	OD60
R/W	R/W	R/W	R/W	R/W	R/W	0	R/W

Bits 7~2, 0 (OD67~OD62,OD60): Open-Drain control bits

0: Disable open-drain function

1: Enable open-drain function

Bit 1: Not used. Set to "**0**" all the time.

6.1.53 Bank 1 R13: P78ODCR (Ports 7~8 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	P8LOD	-	P7LOD
-	-	-	-	-	R/W	0	R/W

Bits 7~3, 1: Not used. Set to "**0**" all the time.

Bit 2 (P8LOD): Control bit used to enable open-drain of Port 8 low nibble pin

0: Disable open-drain function

1: Enable open-drain function

Bit 0 (P7LOD): Control bit used to enable open-drain of Port 7 low nibble pin

6.1.54 Bank 1 R14 ~ R15: (Reserved)

6.1.55 Bank 1 R16: PWMSCR (PWM Source Clock Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	PWM2S	PWM1S
-	-	-	-	-	-	R/W	R/W

Bits 7~2: Not used. Set to "**0**" all the time.

Bit 1 (PWM2S): Clock selection for PWM2 timer

0: Fs (default)

1: Fm

Bit 0 (PWM1S): Clock selection for PWM1 timer

0: Fs (default)

1: Fm

6.1.56 Bank 1 R17: PWM1CR (PWM1 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1E	-	-	-	T1EN	T1P2	T1P1	T1P0
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (PWM1E): PWM1 enable bit

0: Disable (default)

1: Enable. The compound pin is used as PWM1 pin

Bits 6~4: Not used. Set to **"0"** all the time.

Bit 3 (T1EN): TMR1 enable bit. All PWM functions are valid only when this bit is set.

> **NOTE**
> *When the PWM waveform is on, a time delay of 1.5~2.5 PWM clock will occur before PWM output starts.*

0: TMR1 is off (default value)

1: TMR1 is on

PWMXEN	TXEN	Function Description
0	0	Not used as PWM function, I/O pin, or as any other pin function.
0	1	Timer function, I/O pin, or other pin function
1	0	PWM function, the waveform is kept at low level.
1	1	PWM function, normal PWM output waveform

Bits 2~0 (T1P2~T1P0):TMR1 clock prescale option bits

T1P2	T1P1	T1P0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.57 Bank 1 R18: PRD1L (Low Byte of PWM1 Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRD1[7~0]): The contents of the register are the low byte of the PWM1 period.

> **NOTE**
> *If the PWM1 duty/period needs to reload, the PRD1L register must be updated.*

6.1.58 Bank 1 R19: PRD1H (High Byte of PWM1 Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1[F]	PRD1[E]	PRD1[D]	PRD1[C]	PRD1[B]	PRD1[A]	PRD1[9]	PRD1[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRD1[F~8]): The contents of the register are the high byte of the PWM1 period

6.1.59 Bank 1 R1A: DT1L (Low Byte of PMW1 Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT1[7]	DT1[6]	DT1[5]	DT1[4]	DT1[3]	DT1[2]	DT1[1]	DT1[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DT1[7~0]): The contents of the register are the low byte of the PWM1 duty.

6.1.60 Bank 1 R1B: DT1H (High Byte of PMW1 Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT1[F]	DT1[E]	DT1[D]	DT1[C]	DT1[B]	DT1[A]	DT1[9]	DT1[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DT1[F~8]): The contents of the register are the high byte of the PWM1 duty.

6.1.61 Bank 1 R1C: TMR1L (Low Byte of Timer 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR1[7]	TMR1[6]	TMR1[5]	TMR1[4]	TMR1[3]	TMR1[2]	TMR1[1]	TMR1[0]
R	R	R	R	R	R	R	R

Bits 7~0 (TMR1[7~0]): The contents of the register are the low byte of the PWM1 timer which is counting. These bits are read-only.

6.1.62 Bank 1 R1D: TMR1H (High Byte of Timer 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR1[F]	TMR1[E]	TMR1[D]	TMR1[C]	TMR1[B]	TMR1[A]	TMR1[9]	TMR1[8]
R	R	R	R	R	R	R	R

Bits 7~0 (TMR1[F~8]): The contents of the register are the high byte of the PWM1 timer which is counting. These bits are read-only.

6.1.63 Bank 1 R1E: PWM2CR (PWM2 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2E	-	-	-	T2EN	T2P2	T2P1	T2P0
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (PWM2E): PWM2 enable bit

0: Disable (default)

1: Enable. The compound pin is used as PWM2 pin

Bits 6~4: Not used. Set to "**0**" all the time.

Bit 3 (T2EN): TMR2 enable bit. All PWM functions are valid only after this bit is set.

> **NOTE**
> *When the PWM waveform is on, a time delay of 1.5~2.5 PWM clock will occur before PWM output starts.*

0: TMR2 is off (default value)

1: TMR2 is on

Bits 2~0 (T2P2~T2P0): TMR2 clock prescale option bits

T2P2	T2P1	T2P0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.64 Bank 1 R1F: PRD2L (Low Byte of PWM2 Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRD2[7~0]): The contents of the register are the low byte of the PWM2 period.

> **NOTE**
> *If the PWM2 duty/period needs to reload, the PRD2L register must be updated.*

6.1.65 Bank 1 R20: PRD2H (High Byte of PWM2 Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2[F]	PRD2[E]	PRD2[D]	PRD2[C]	PRD2[B]	PRD2[A]	PRD2[9]	PRD2[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRD2[F~8]): The contents of the register are the high byte of the PWM2 period.

6.1.66 Bank 1 R21: DT2L (Low Byte of PMW2 Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT2[7]	DT2[6]	DT2[5]	DT2[4]	DT2[3]	DT2[2]	DT2[1]	DT2[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DT2[7~0]): The contents of the register are the low byte of the PWM2 duty.

6.1.67 Bank 1 R22: DT2H (High Byte of PMW2 Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT2[F]	DT2[E]	DT2[D]	DT2[C]	DT2[B]	DT2[A]	DT2[9]	DT2[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DT2[F~8]): The contents of the register are the high byte of the PWM2 duty.

6.1.68 Bank 1 R23: TMR2L (Low Byte of Timer 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR2[7]	TMR2[6]	TMR2[5]	TMR2[4]	TMR2[3]	TMR2[2]	TMR2[1]	TMR2[0]
R	R	R	R	R	R	R	R

Bits 7~0 (TMR2[7~0]): The contents of the register are the low byte of the PWM2 timer which is counting. These bits are read-only.

6.1.69 Bank 1 R24: TMR2H (High Byte of Timer 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR2[F]	TMR2[E]	TMR2[D]	TMR2[C]	TMR2[B]	TMR2[A]	TMR2[9]	TMR2[8]
R	R	R	R	R	R	R	R

Bits 7~0 (TMR2[F~8]): The contents of the register are the high byte of the PWM2 timer which is counting. These bits are read-only

6.1.70 Bank 1 R25 ~ R44: (Reserved)

6.1.71 Bank 1 R45: TBPTL (Table Point Low Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TB7~TB0): Table Point Address Bits 7~0.

6.1.72 Bank 1 R46: TBPTH (Table Point High Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	RDS	-	TB12	TB11	TB10	TB9	TB8
R/W	R/W	0	R/W	R/W	R/W	R/W	R/W

Bit 7 (HLB): Obtain MLB or LSB at machine code of ROM or Data area.

RDS	HLB	Read to Register Data Value Description
0	**0**	Read byte value is Bit 7 ~ Bit 0 from machine code.
0	**1**	Read byte value is– Highest bit fixed at “**0**” and Bit 14 ~ Bit 8 from machine code.
1	**0**	Read byte value is Bit 7 ~ Bit 0 from Data area.
1	**1**	Read byte value is Bit 15~Bit 8 from Data area.

Bit 6 (RDS): ROM / Data select bit, read machine code information area select.

0: ROM (default)

1: Data area (data Address 000~17F)

Bit 5: Not used. Set to “**0**” all the time.

Bits 4~0 (TB12~TB8): Table point Address Bits 12~8.

6.1.73 Bank 1 R47: STKMON (Stack Pointer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STOF	-	-	-	-	STL2	STL1	STL0
R	-	-	-	-	R	R	R

Bit 7(STOF): Stack pointer overflow indicator bit. Read only.

Bits 2~0 (STL2~0): Stack pointer number. Read only.

6.1.74 Bank 1 R48: PCH (Program Counter High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	PC12	PC11	PC10	PC9	PC8
-	-	-	R/W	R/W	R/W	R/W	R/W

Bits 7~5: Not used. Set to “**0**” all the time.

Bits 4~0 (PC12~PC8): The high byte of program counter

6.1.75 Bank 1 R49~ R4F: (Reserved)

6.1.76 Bank 2 R5 TPEPCR1 (Touch Pad Groups A&B Enable Pin Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPAEP3	TPAEP2	TPAEP1	-	TPBEP3	TPBEP2	TPBEP1	-
R/W	R/W	R/W	0	R/W	R/W	R/W	0

Bit 7 (TPAEP3): Touch Pad Enable Pin Control Bits

0: P62/TPSA3 is P62 pin.

1: Functions as Touch Pad pin, TPSA3 is TP Sensor or Self function pin.

Bit 6 (TPAEP2): Touch Pad Enable Pin Control Bits

0: P64/TPSA2 is P64 pin.

1: Functions as Touch Pad pin, TPSA2 is TP Sensor or Self function pin.

Bit 5 (TPAEP1): Touch Pad Enable Pin Control Bits

0: P50//SS/TPSA1 is P50//SS pin.

1: Functions as Touch Pad pin, TPSA1 is TP Sensor or Self function pin.

Bit 4: Not used, set to "0" all the time.

Bit 3 (TPBEP3): Touch Pad Enable Pin Control Bits

0: P63/TPSB3 is P63 pin.

1: Functions as Touch Pad pin, TPSB3 is TP Sensor or Self function pin.

Bits 2 (TPBEP2): Touch Pad Enable Pin Control Bits

0: P65/TPSB2 is P65 pin.

1: Functions as Touch Pad pin, TPSB2 is TP Sensor or Self function pin.

Bits 1 (TPBEP1): Touch Pad Enable Pin Control Bits

0: P51/SO/TPSB1 is P51/SO pin.

1: Functions as Touch Pad pin, TPSB1 is TP Sensor or Self function pin.

Bit 0: Not used, set to "0" all the time.

6.1.77 Bank 2 R6 TPEPCR2 (Touch Pad Groups C&D Enable Pin Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPCEP3	TPCEP2	TPCEP1	-	TPDEP3	TPDEP2	TPDEP1	-
R/W	R/W	R/W	0	R/W	R/W	R/W	0

Bit 7 (TPCEP3): Touch Pad Enable Pin Control Bits

0: P72/PWM1/TPSC3 is P72/PWM1 pin.

1: Functions as Touch Pad pin, TPSC3 is TP Sensor or Self function pin.

Bit 6 (TPCEP2): Touch Pad Enable Pin Control Bits

0: P66/TPSC2 is P66 pin.

1: Functions as Touch Pad pin, TPSC2 is TP Sensor or Self function pin.

Bit 5 (TPCEP1): Touch Pad Enable Pin Control Bits

0: P52/SI/TPSC1 is P52/SI pin.

1: Functions as Touch Pad pin, TPSC1 is TP Sensor or Self function pin.

Bit 4: Not used, set to "0" all the time.

Bit 3 (TPDEP3): Touch Pad Enable Pin Control Bits

0: P73/PWM2/TPSD3 is P73/PWM2 pin.

1: Functions as Touch Pad pin, TPSD3 is TP Sensor or Self function pin.

Bit 2 (TPDEP2): Touch Pad Enable Pin Control Bits

0: P67/TPSD2 is P67 pin.

1: Functions as Touch Pad pin, TPSD2 is TP Sensor or Self function pin.

Bit 1 (TPDEP1): Touch Pad Enable Pin Control Bits

0: P53/SCK/TPSD1 is P53/SCK pin.

1: Functions as Touch Pad pin, TPSD1 is TP Sensor or Self function pin.

Bit 0: Not used, set to "0" all the time.

6.1.78 Bank 2 R7 TPEPCR3 (Touch Pad Drive Enable Pin Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPDE7	TPDE6	TPDE5	TPDE4	-	-	-	-
R/W	R/W	R/W	R/W	0	0	0	0

Bit 7 (TPDE7): Touch Pad Drive pin Enable Control Bits

0: P83/TPD7/TPSD0 is P83/TPSD0 pin.

1: Touch Pad Drive pin Enable, TPD7 is TP Drive function pin.

Bit 6 (TPDE6): Touch Pad Drive pin Enable Control Bits

0: P55/TPD6/TPSC0 is P55/TPSC0 pin.

1: Touch Pad Drive pin Enable, TPD6 is TP Drive function pin

Bit 5 (TPDE5): Touch Pad Drive pin Enable Control Bits

0: P57/DA1/TPD5/TPSB0 is P57/DA1/TPSB0 pin.

1: Touch Pad Drive pin Enable, TPD5 is TP Drive function pin

Bit 4 (TPDE4): Touch Pad Drive pin Enable Control Bits

0: P56/DA0/TPD4/TPSA0 is P56/DA0/TPSA0 pin.

1: Touch Pad Drive pin Enable, TPD4 is TP Drive function pin

Bits 3~0: Not used, set to "0" all the time.

6.1.79 Bank 2 R8 TPCR1 (Touch Pad Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	TPICS	TPS	-	-	-
1	0	0	R/W	R/W	1	1	0

Bits 7, 2~1: Not used, set to "1" all the time.

Bits 6~5, 0: not used bits, fixed to “0” all the time.

Bit 4 (TPICS): TP Integration Capacitor Select

0: 5pf

1: 10pf

Bit 3 (TPS): TP Conversion Start Bit

0: Reset on completion of the conversion by hardware, this bit cannot be reset by software.

1: Conversion start

6.1.80 Bank 2 RA TPDCR (Touch Pad Drive Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPDWO[7]	TPDWO[6]	TPDWO[5]	TPDWO[4]	-	-	-	-
R/W	R/W	R/W	R/W	0	0	0	0

Bits 7~4 (TPDWO[7]~TPDWO[4]): Touch Pad Drive Waveform Output control bits

0 : Short to GND.

1 : Touch Pad Drive waveform output enable,

Bits 3~0: not used bits, fixed to "0" all the time.

6.1.81 Bank 2 RB TPASCR (Touch Pad Group A Sensor Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPAEN	-	-	-	-	-	TPASW1	TPASW0
R/W	0	0	0	0	0	R/W	R/W

Bit 7 (TPAEN): Touch Pad Group A Enable Bit (TP must operating in Normal mode)

0: Disable.

1: Enable.

Bit 6~2: not used bits, fixed to "0" all the time.

Bits 1~0 (TPASW1~TPASW0): Touch Pad Switch Bits.

TPxSW1	TPxSW0	Function
0	0	TPSx1, TPSx2 and TPSx3 all off
0	1	TPSx1 is sensor pin TPSx2 and TPSx3 off
1	0	TPSx2 is sensor pin TPSx1 and TPSx3 off
1	1	TPSx3 is sensor pin TPSx1 and TPSx2 off

*x = A, B, C

6.1.82 Bank 2 RC TPBSCR (Touch Pad Group B Sensor Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPBEN	-	-	-	-	-	TPBSW1	TPBSW0
R/W	0	0	0	0	0	R/W	R/W

Bit 7 (TPBEN): Touch Pad Group B Enable Bit (TP must operating in Normal mode)

0: Disable.

1: Enable.

Bit 6~2 : not used bits, fixed to "0" all the time.

Bits 1~0 (TPBSW1~TPBSW0): Touch Pad Switch Bits.

Bank2 RD TPCSCR (Touch Pad Group C Sensor Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPCEN	-	-	-	-	-	TPCSW1	TPCSW0
R/W	0	0	0	0	0	R/W	R/W

Bit 7 (TPCEN): Touch Pad Group C Enable Bit (TP must operating in Normal mode)
0: Disable.
1: Enable.

Bit 6~2 : not used bits, fixed to “0” all the time.

Bits 1~0 (TPCSW1~TPCSW0): Touch Pad Switch Bits.

Bank2 RE TPDSCR (Touch Pad Group D Sensor Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPDEN	-	-	-	-	-	TPDSW1	TPDSW0
R/W	0	0	0	0	0	R/W	R/W

Bit 7 (TPDEN): Touch Pad Group D Enable Bit (TP must operating in Normal mode)
0: Disable.
1: Enable.

Bits 6~2 : not used bits, fixed to “0” all the time.

Bits 1~0 (TPDSW1~TPDSW0): Touch Pad Switch Bits.

Bank2 R10 GADCCR (Group A Discharge Current Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	GADCS4	GADCS3	GADCS2	GADCS1	-
0	0	0	R/W	R/W	R/W	R/W	0

Bit 7~5,0 : not used bits, fixed to “0” all the time.

Bit 4~1 (GADCS4~GADCS1): Group x Discharge Current Source select Bits.

GxDCS4	GxDCS3	GxDCS2	GxDCS1	Current
0	0	0	1	0.25uA
0	0	1	0	0.5uA
0	1	0	0	1uA
1	0	0	0	2uA
1	1	1	1	3. 75uA

*x = A, B, C, D

Bank2 R11 GBDCCR (Group B Discharge Current Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	GBDCS4	GBDCS3	GBDCS2	GBDCS1	-
0	0	0	R/W	R/W	R/W	R/W	0

Bit 7~5,0 : not used bits, fixed to “0” all the time.

Bit 4~1 (GBDCS4~GBDCS1): Group B Discharge Current Source select Bits.

Bank2 R12 GCDCCR (Group C Discharge Current Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	GCDCS4	GCDCS3	GCDCS2	GCDCS1	-
0	0	0	R/W	R/W	R/W	R/W	0

Bit 7~5,0 : not used bits, fixed to “0” all the time.

Bit 4~1 (GCDCS4~GCDCS1): Group C Discharge Current Source select Bits.

Bank2 R13 GDDCCR (Group D Discharge Current Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	GDDCS4	GDDCS3	GDDCS2	GDDCS1	-
0	0	0	R/W	R/W	R/W	R/W	0

Bit 7~5,0 : not used bits, fixed to “0” all the time.

Bit 4~1 (GDDCS4~GDDCS1): Group D Discharge Current Source select Bits.

Bank2 R18 TPSPCR (Touch Pad Sampling Cycle control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPCY7	SPCY6	SPCY5	SPCY4	SPCY3	SPCY2	SPCY1	SPCY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (SPCY7~SPCY0): Touch Pad sampling cycle set for one trace.

Touch Pad Sampling Cycle time = (TPSPCR + 1)

Bank2 R19 TPAH (The Most Significant Byte of A Group Touch Pad Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

TPA[15]	TPA[14]	TPA[13]	TPA[12]	TPA[11]	TPA[10]	TPA[9]	TPA[8]
R	R	R	R	R	R	R	R

Bits 7~0 (TPA [15]~TPA[8]): The Most Significant Byte of A Group Touch Pad Buffer.

Bank2 R1A TPAL (The Least Significant Byte of A Group Touch Pad Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPA[7]	TPA[6]	TPA[5]	TPA[4]	TPA[3]	TPA[2]	TPA[1]	TPA[0]
R	R	R	R	R	R	R	R

Bits 7~0 (TPA[7]~TPA[0]): The Least Significant Byte of A Group Touch Pad Buffer.

Bank2 R1B TPBH (The Most Significant Byte of B Group Touch Pad Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPB[15]	TPB[14]	TPB[13]	TPB[12]	TPB[11]	TPB[10]	TPB[9]	TPB[8]
R	R	R	R	R	R	R	R

Bits 7~0 (TPB[15]~TPB[8]): The Most Significant Byte of B Group Touch Pad Buffer.

Bank2 R1C TPBL (The Least Significant Byte of B Group Touch Pad Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPB[7]	TPB[6]	TPB[5]	TPB[4]	TPB[3]	TPB[2]	TPB[1]	TPB[0]
R	R	R	R	R	R	R	R

Bits 7~0 (TPB[7]~TPB[0]): The Least Significant Byte of B Group Touch Pad Buffer.

Bank2 R1D TPCH (The Most Significant Byte of C Group Touch Pad Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPC[15]	TPC[14]	TPC[13]	TPC[12]	TPC[11]	TPC[10]	TPC[9]	TPC[8]
R	R	R	R	R	R	R	R

Bits 7~0 (TPC[15]~TPC[8]): The Most Significant Byte of C Group Touch Pad Buffer.

Bank2 R1E TPCL (The Least Significant Byte of C Group Touch Pad Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPC[7]	TPC[6]	TPC[5]	TPC[4]	TPC[3]	TPC[2]	TPC[1]	TPC[0]
R	R	R	R	R	R	R	R

Bits 7~0 (TPC[7]~TPC[0]): The Least Significant Byte of C Group Touch Pad Buffer.

Bank2 R1F TPDH (The Most Significant Byte of D Group Touch Pad Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPD[15]	TPD[14]	TPD[13]	TPD[12]	TPD[11]	TPD[10]	TPD[9]	TPD[8]
R	R	R	R	R	R	R	R

Bits 7~0 (TPD[15]~TPD[8]): The Most Significant Byte of D Group Touch Pad Buffer.

Bank2 R20 TPDL (The Least Significant Byte of D Group Touch Pad Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPD[7]	TPD[6]	TPD[5]	TPD[4]	TPD[3]	TPD[2]	TPD[1]	TPD[0]
R	R	R	R	R	R	R	R

Bits 7~0 (TPD[7]~TPD[0]): The Least Significant Byte of D Group Touch Pad Buffer.

Bank2 R21 DACR (DAC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						DAE1	DAE0
						R/W	R/W

Bits 7~2 : not used bits, fixed to “0” all the time.

Bits 1 (DAE1): DAC enable bit of P57 pin.

0: Disable DA1, P57 act as I/O pin.

1: Enable DA1 act as analog output pin.

Bits 0 (DAE0): DAC enable bit of P56 pin.

0: Disable DA0, P56 act as I/O pin.

1: Enable DA0 act as analog output pin.

6.1.80 Bank 2 R21: DACR (DAC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	DAE1	DAE0
-	-	-	-	-	-	R/W	R/W

Bits 7~2: Not used. Set to “**0**” all the time.

Bits 1 (DAE1): DAC enable bit of P57 pin

0: Disable DA1/P57 serving as I/O pin

1: Enable DA1/P57 serving as analog output pin

Bits 0 (DAE0): DAC enable bit of P56 pin

0: Disable DA0/P56 serving as I/O pin

1: Enable DA0/P56 serving as analog output pin

6.1.81 Bank 2 R22: DACD0 (Digital-to-Analog Converter Data Buffer 0)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAD0[7]	DAD0[6]	DAD0[5]	DAD0[4]	DAD0[3]	DAD0[2]	DAD0[1]	DAD0[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DAD0[7]~DAD0[0]): DA0 Data buffer

6.1.82 Bank 2 R23: DACD1 (Digital-to-Analog Converter Data Buffer 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAD1[7]	DAD1[6]	DAD1[5]	DAD1[4]	DAD1[3]	DAD1[2]	DAD1[1]	DAD1[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DAD1[7]~DAD1[0]): DA1 Data Buffer.

6.1.83 Bank 2 R25 ~ R4F: (Reserved)

6.1.84 R50~R7F, Banks 0~3 R80~RFF

These are all 8-bit general-purpose registers.

6.2 TCC/WDT and Prescaler

Two 8-bit counters are available as prescalers for the TCC and WDT respectively. The TPSR0~ TPSR2 bits of the TCCCR register (Bank0 R22) are used to determine the ratio of the TCC prescaler. Likewise, the WPSR0~WPSR2 bits of the WDTCR register (Section 6.1.25*Bank 0 R21*) are used to determine the WDT prescaler. The prescaler counter is cleared by the instructions each time they are written into TCC. The WDT and prescaler are cleared by the "WDTC" and "SLEP" instructions. Figure 6-3 below depicts the circuit diagram of TCC/WDT.

TCCD (Section 6.1.27*Bank 0 R23*) is an 8-bit timer/counter. The TCC clock source is from the internal clock only and TCC will increase by 1 at Fc clock (without prescaler). **The TCC will stop running when Sleep mode occurs.**

The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e., in Sleep mode). During Normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during Normal mode by software programming (see WDTE bit of WDTCR (Section 6.1.25*Bank 0 R21*) register). With no prescaler, the WDT time-out period is approximately 18 ms[5] (one oscillator start-up timer period).

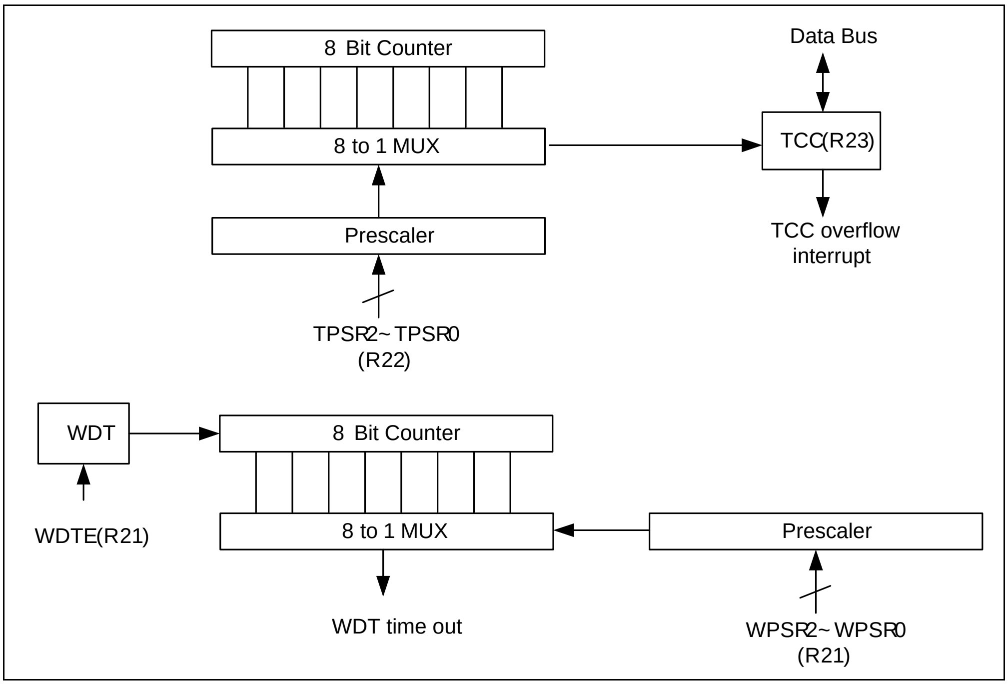


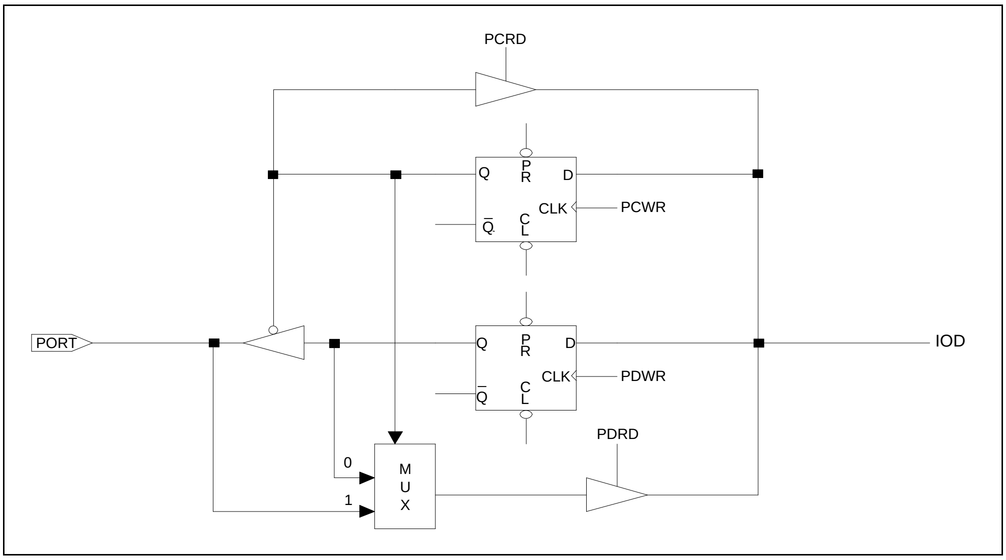
Figure 6-3 TCC and WDT Block Diagram

[5] *VDD=5V, WDT time-out period = 16.5ms ± 8%.*
VDD=3V, WDT time-out period = 18ms ± 8%.

6.3 I/O Ports

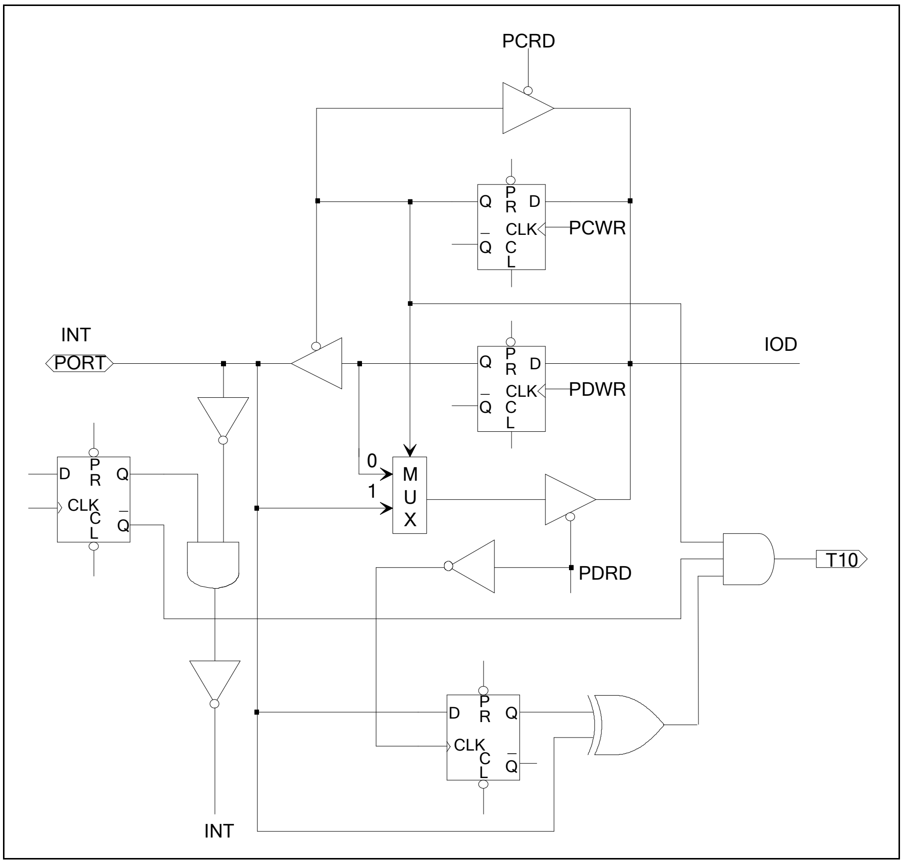
The I/O registers, Port 5~Port 8 are bidirectional tri-state I/O ports. All can be pulled high and pulled low internally by software. Furthermore, they can also be set as open-drain output and high sink/drive by software. Ports 5~8 feature wake-up and interrupt function as well as input status change interrupt function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC8).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 ~ Port 8 are shown in the following Figure 6-4a to 6-4d.



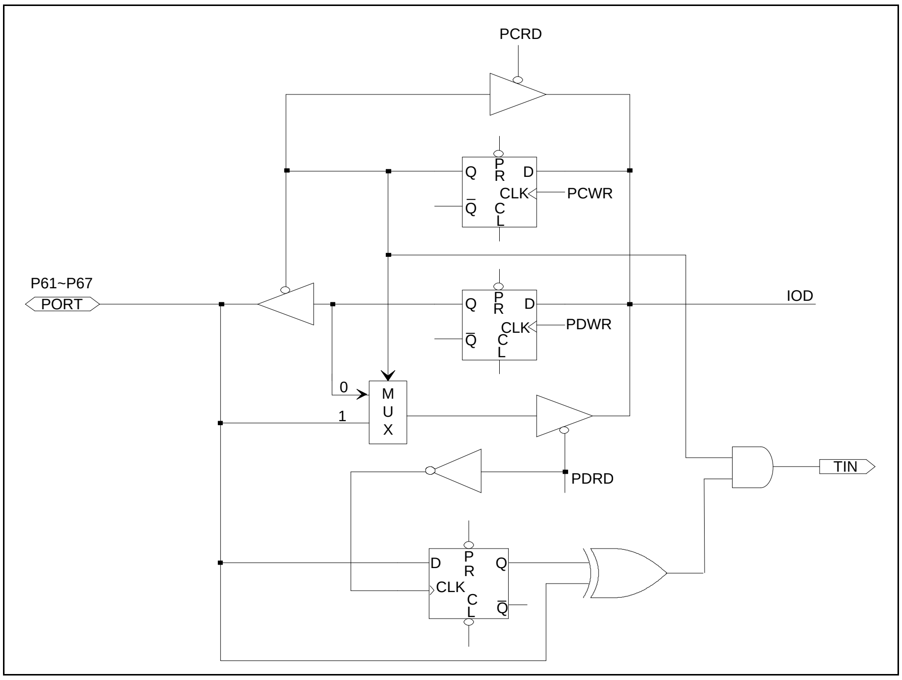
Note: *Pull-down is not shown in the figure.*

Figure 6-4a I/O Port and I/O Control Register for Port 5~8 Circuit Diagram



***Note:** Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-4b I/O Port and I/O Control Register for /INT Circuit



***Note:** Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-4c I/O Port and I/O Control Register for Ports 5~8 Circuit

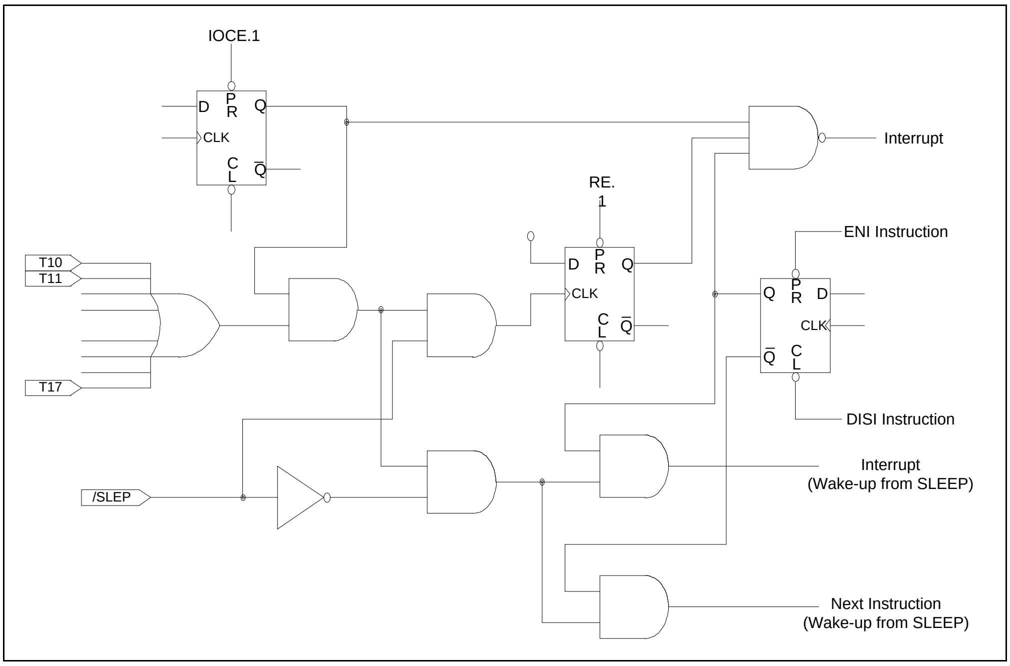


Figure 6-4d I/O Port 5~8 with Input Change Interrupt/Wake-up Block Diagram

6.3.1 Usage of Ports 5~8 Input Change Wake-up/Interrupt Function

1. Wake-up
a) Before Sleep:
1) Disable WDT
2) Read I/O Port (MOV R6,R6)
3) Execute "ENI" or "DISI"
4) Enable Wake-up bit (Set **ICWKPx** = 1)
5) Execute "SLEP" instruction
b) After Wake-up:
→ Next instruction

2. Wake-up and Interrupt
a) Before SLEEP
1) Disable WDT
2) Read I/O Port (MOV R6,R6)
3) Execute "ENI" or "DISI"
4) Enable Wake-up bit (Set **ICWKPx** = 1)
5) Enable interrupt (Set PxICIE = 1)
6 Execute "SLEP" instruction
b) After Wake-up
1) IF "ENI" → Interrupt vector (0006H)
2) IF "DISI" → Next instruction

6.4 Reset and Wake-up

A Reset is initiated by one of the following events:

1) Power-on reset
2) /RESET pin input "low"
3) WDT time-out (if enabled)
4) LVR (if enabled)

The device is kept in a Reset condition for a period of approximately 18ms[6] (one oscillator start-up timer period) after a reset is detected. And if the /Reset pin goes “low” or the WDT time-out is active, a reset is generated. In IRC mode, the reset time is 8/32 clocks. Once a Reset occurs, the following functions are performed (see Figure 6-5 below):

- The oscillator continuous running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog Timer and prescaler are cleared.
- The control register bits are set as shown in the table below under Section 6.4.3, *Summary of Register Initial Values after Reset*.

The Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering Sleep mode, WDT (if enabled) is cleared but keeps on running. Wake-up is then generated (in IRC mode the wake-up time is 8/32 clocks). The controller can be awakened by any of the following events:

1) External reset input on /RESET pin
2) WDT time-out (if enabled)
3) External (/INT) pin changes (if INTWE is enabled)
4) Port input status changes (if ICWKPx is enabled)
5) SPI receives data while it serves as Slave device (if SPIWK is enabled)
6) I^2C receives data while it serves as Slave device (if I2CWK is enabled)
7) A/D conversion completed (if ADWK is enabled)

The first two events (1 and 2) will cause the eKTF5705 to reset. The T and P flags of R3 are used to determine the source of the reset (Wake-up). Events 3 to 7 are considered as continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following Wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x02~0x3C after Wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after Wake-up.

[6] Vdd = 5V, set up time period = 16.8ms ± 8%
Vdd = 3V, set up time period = 18ms ± 8%

Only one of Events 3 to 7 can be enabled before entering into Sleep mode. That is:

a) If WDT is enabled before SLEP, the eKTF5705 can wake-up only when Events 1 or 2 occurs. Refer to the Section 6.5 *Interrupt*, for further details.

b) If External (P60, /INT) pin change is used to wake-up eKTF5705 and EXWE bit is enabled before SLEP (with WDT disabled). Hence, the eKTF5705 can wake-up only when Event 3 occurs.

c) If Port Input Status Change is used to wake-up eKTF5705 and the corresponding wake-up setting is enabled before SLEP (with WDT disabled). Hence, the eKTF5705 can wake-up only when Event 4 occurs.

d) With SPI serving as Slave device and the SPIWK bit of Bank0 R11 register is enabled before SLEP (with WDT disabled), the SPI will wake-up eKTF5705 after it receives data. Hence, the eKTF5705 can wake-up only when Event 5 occurs.

e) When I^2C serving as Slave device and I2CWK bit of Bank0 R11 register is enabled before SLEP (with WDT disabled), the I^2C will wake-up eKTF5705 after it received data. Hence, the eKTF5705 can be wake-up only by Event 6.

6.4.1 Summary of Wake-up and Interrupt Mode Operation

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
External INT	INTWK = 0, EXIE = 0	/INT pin Disable							
	INTWK = 0, EXIE = 1	Wake-up is invalid				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	INTWK = 1, EXIE = 0	/INT pin Disable							
	INTWK = 1, EXIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TCC INT	TCIE = 0	Wake-up is invalid				Interrupt is invalid			
	TCIE = 1	Wake-up is invalid		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWM1/2 (When Timer1/2 Match PRD1/2)	PWMXPIE=0	Wake-up is invalid				Interrupt is invalid			
	PWMxPIE=1	Wake-up is invalid		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

(Continuation)

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
Pin Change INT	ICWKPx = 0 PxICIE = 0	Wake-up is invalid				Interrupt is invalid			
	ICWKPx = 0 PxICIE = 1	Wake-up is invalid				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWKPx = 1 PxICIE = 0	Wake up + Next Instruction				Interrupt is invalid			
	ICWKPx = 1 PxICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
I^2C INT	I2CWK = 0 I2CxIE = 0	Wake-up is invalid				I^2C Can't be used		Interrupt is invalid	
	I2CWK = 0 I2CxIE = 1	Wake-up is invalid				I^2C Can't beused		Next Instruction	Interrupt + Interrupt Vector
	I2CWK = 1, I2CxIE = 0	Wake up + Next Instruction **I^2C must be in Slave mode**				I^2C Can't be used		Interrupt is invalid	
	I2CWK = 1 I2CxIE = 1	Wake up + Next Instruction **I^2C must be in Slave mode**	Wake up + Interrupt Vector **I^2C must be in Slave mode**	Wake up + Next Instruction **I^2C must be in Slave mode**	Wake up + Interrupt Vector **I^2C must be in Slave mode**	I^2C Can't be used		Next Instruction	Interrupt + Interrupt Vector
SPI INT	SPIWK = 0 SPIE = 0	Wake-up is invalid				Interrupt is invalid			
	SPIWK = 0 SPIE = 1	Wake-up is invalid				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	SPIWK = 1 SPIE = 0	Wake up + Next Instruction **SPI must be in Slave mode**				Interrupt is invalid			
	SPIWK = 1 SPIE = 1	Wake up + Next Instruction **SPI must be in Slave mode**	Wake up + Interrupt Vector **SPI must be in Slave mode**	Wake up + Next Instruction **SPI must be in Slave mode**	Wake up + Interrupt Vector **SPI must be in Slave mode**	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

(Continuation)

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
WDT time out	–	RESET	RESET	RESET	RESET	RESET	RESET	RESET	RESET

NOTE

After wake up:

1. If interrupt enable → interrupt+ next instruction

2. If interrupt disable → next instruction

6.4.2 The Status of RST, T, and P of Status Register

A reset condition is initiated by one of the following events**:**

1) Power-on condition
2) High-low-high pulse on the /RESET pin
3) Watchdog timer time-out
4) When LVR occurs

The values of T and P, as listed in the following table are used to check how the MCU wakes up. The next table shows the events that may affect the status of T and P.

■ **Values of RST, T and P after Reset:**

Reset Type	T	P
Power-on	1	1
/RESET during Operating mode	P*	P*
/RESET Wake-up during Sleep mode	1	0
WDT during Operating mode	0	P*
WDT Wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

* ***P:** Previous status before reset*

■ **Status of T and P being affected by Events:**

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

* ***P:** Previous value before reset*

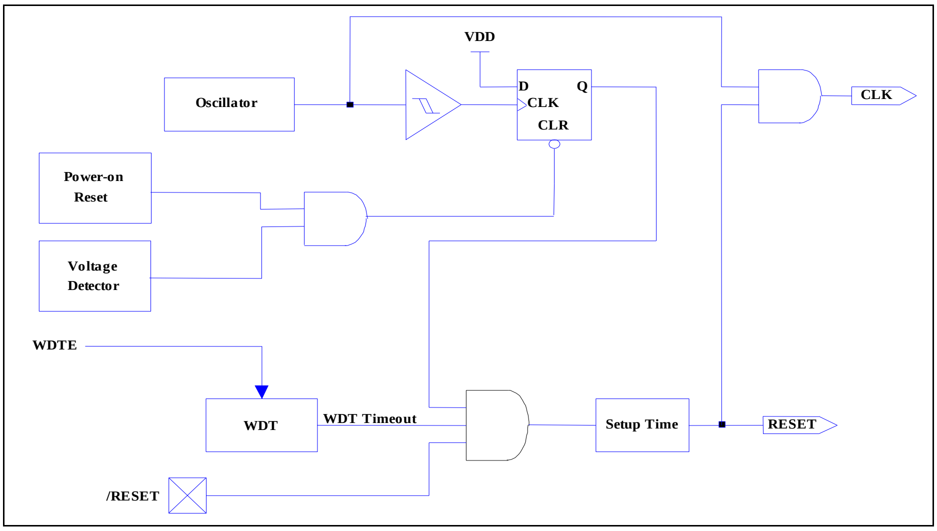


Figure 6-5 Block Diagram of Controller Reset

6.4.3 Summary of Register Initial Values after Reset

Legend: ***U:*** *Unknown or don't care* ***P:*** *Previous value before reset*
C: *Same with Code option* ***t:*** *Check tables under Section 6.4.2*

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x01	R1 (BSR)	Bit Name	0	0	SBS1	SBS0	0	GBS2	GBS1	GBS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	0	P	P	P
0x02	R2 (PCL)	Bit Name	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x03	R3 (SR)	Bit Name	INT	0	0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Sleep/Idle	P	0	0	t	t	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x04	R4 (RSR)	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X05	Bank 0, R5 (Port 5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x06	Bank 0, R6 (Port 6)	Bit Name	-	P66	P65	P64	P63	P62	-	P60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	P	P	P	P	P	0	P
0x07	Bank 0, R7 (Port 7)	Bit Name	-	-	-	-	P73	P72	P71	P70
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0x08	Bank 0, R8 (Port 8)	Bit Name	-	-	-	-	P83	-	-	P80
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	0	0	P
0X0B	Bank 0, RB (IOCR5)	Bit Name	IOC57	IOC56	IOC55	IOC54	IOC53	IOC52	IOC51	IOC50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x0C	Bank 0, RC (IOCR6)	Bit Name	-	IOC66	IOC65	IOC64	IOC63	IOC62	-	IOC60
		Power-on	0	1	1	1	1	1	0	1
		/RESET and WDT	0	1	1	1	1	1	0	1
		Wake-up from Sleep/Idle	0	P	P	P	P	P	0	P
0X0D	Bank 0, RD (IOCR7)	Bit Name	-	-	-	-	IOC73	IOC72	IOC71	IOC70
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0E	Bank 0, RE (OMCR)	Bit Name	CPUS	IDLE	-	-	-	-	RCM1	RCM0
		Power-on	Code option	1	0	0	0	0	Code option	Code option
		/RESET and WDT	Code option	1	0	0	0	0	Code option	Code option
		Wake-up from Sleep/Idle	P	P	0	0	0	0	P	P
0X0F	Bank 0, RF EIESCR	Bit Name	-	-	-	-	-	EIES	-	-
		Power-on	0	0	0	0	0	1	0	0
		/RESET and WDT	0	0	0	0	0	1	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	P	0	0
0x10	Bank 0, R10 (WUCR1)	Bit Name	-	-	-	-	-	INTWK	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	P	0	P	0	0
0x11	Bank 0, R11 WUCR2	Bit Name	-	-	-	-	SPIWK	I2CWK	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	0	0
0x12	Bank 0, R12 WUCR3	Bit Name	ICWKP8	ICWKP7	ICWKP6	ICWKP5	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	0	0	0	0
0X14	Bank 0, R14 SFR1	Bit Name	-	-	-	-	-	EXSF	-	TCSF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	P	0	P
0X16	Bank 0, R16 SFR3	Bit Name	-	-	-	-	PWM2P SF	PWM2D SF	PWM1P SF	PWM1D SF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X17	Bank 0, R17 SFR4	Bit Name	P8ICSF	P7ICSF	P6ICSF	P5ICSF	SPISF	I2CSTP SF	I2CRSF	I2CTSF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1B	Bank 0, R1B IMR1	Bit Name	-	-	-	-	-	EXIE	-	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	0	0
0X1D	Bank 0, R1D IMR3	Bit Name	-	-	-	-	PWM2 PIE	PWM2 DIE	PWM1 PIE	PWM1 DIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X1E	Bank 0, R1E IMR4	Bit Name	P8ICIE	P7ICIE	P6ICIE	P5ICIE	SPIIE	I2CSTPIE	I2CRIE	I2CTIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X21	Bank 0, R21 WDTCR	Bit Name	WDTE	-	-	-	PSWE	WPSR2	WPSR1	WPSR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	P	P	P	P
0X22	Bank 0, R22 TCCCR	Bit Name	-	TCCS	-	-	PSTE	TPSR2	TPSR1	TPSR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	P	0	0	P	P	P	P
0X23	Bank 0, R23 TCCD	Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X30	Bank 0, R30 I2CCR1	Bit Name	Strobe/ Pend	IMS	ISS	STOP	SAR_ EMPTY	ACK	FULL	EMPTY
		Power-on	0	0	0	0	1	0	0	1
		/RESET and WDT	0	0	0	0	1	0	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X31	Bank 0, R31 I2CCR2	Bit Name	I2CBF	GCEN	-	BBF	I2CTS1	I2CTS0	-	I2CEN
		Power-on	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-up from Sleep/Idle	P	P	0	P	P	P	0	P
0X32	Bank 0, R32 I2CSA	Bit Name	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X33	Bank 0, R33 I2CDB	Bit Name	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X34	Bank 0, R34 I2CDAL	Bit Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X35	Bank 0, R35 I2CDAH	Bit Name	-	-	-	-	-	-	DA9	DA8
		Power-on	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X36	Bank 0, R36 SPICR	Bit Name	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X37	Bank 0, R37 SPIS	Bit Name	DORD	TD1	TD0	-	OD3	OD4	-	RBF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X38	Bank 0, R38 SPIR	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X39	Bank 0, R39 SPIW	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X05	Bank 1, R5 IOCR8	Bit Name	-	-	-	-	IOC83	-	-	IOC80
		Power-on	0	0	0	0	1	0	0	1
		/RESET and WDT	0	0	0	0	1	0	0	1
		Wake-up from Sleep/Idle	0	0	0	0	P	0	0	P
0X08	Bank 1, R8 P5PHCR	Bit Name	PH57	PH56	PH55	PH54	PH53	PH52	PH51	PH50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X09	Bank 1, R9 P6PHCR	Bit Name	PH67	PH66	PH65	PH64	PH63	PH62	-	PH60
		Power-on	1	1	1	1	1	1	0	1
		/RESET and WDT	1	1	1	1	1	1	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	0	P
0X0A	Bank 1, RA P78PHCR	Bit Name	-	-	-	-	-	P8LPH	-	P7LPH
		Power-on	0	0	0	0	0	1	0	1
		/RESET and WDT	0	0	0	0	0	1	0	1
		Wake-up from Sleep/Idle	0	0	0	0	0	P	0	P
0X0B	Bank 1, RB P5PLCR	Bit Name	PL57	PL56	PL55	PL54	PL53	PL52	PL51	PL50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0C	Bank 1, RC P6PLCR	Bit Name	PL67	PL66	PL65	PL64	PL63	PL62	-	PL60
		Power-on	1	1	1	1	1	1	0	1
		/RESET and WDT	1	1	1	1	1	1	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	0	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0D	Bank 1, RD P78PLCR	Bit Name	-	-	-	-	-	P8LPL	-	P7LPL
		Power-on	0	0	0	0	0	1	0	1
		/RESET and WDT	0	0	0	0	0	1	0	1
		Wake-up from Sleep/Idle	0	0	0	0	0	P	0	P
0X0E	Bank 1, RE P5HDSCR	Bit Name	H57	H56	H55	H54	H53	H52	H51	H50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0F	Bank 1, RF P6HDSCR	Bit Name	H67	H66	H65	H64	H63	H62	-	H60
		Power-on	1	1	1	1	1	1	0	1
		/RESET and WDT	1	1	1	1	1	1	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	0	P
0X10	Bank 1, R10 P78HDSCR	Bit Name	-	-	-	-		P8LHDS	-	P7LHDS
		Power-on	0	0	0	0	0	1	0	1
		/RESET and WDT	0	0	0	0	0	1	0	1
		Wake-up from Sleep/Idle	0	0	0	0	0	P	0	P
0X11	Bank 1, R11 P5ODCR	Bit Name	OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X12	Bank 1, R12 P6ODCR	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	-	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	0	P
0X13	Bank 1, R13 P78ODCR	Bit Name	-	-	-	-	-	P8LOD	-	P7LOD
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	P	0	P
0X16	Bank 1, R16 PWMSCR	Bit Name	-	-	-	-	-	-	PWM2S	PWM1S
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X17	Bank 1, R17 PWM1CR	Bit Name	PWM1E	-	-	-	T1EN	T1P2	T1P1	T1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	P	P	P	P
0X18	Bank 1, R18 PRD1L	Bit Name	PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X19	Bank 1, R19 PRD1H	Bit Name	PRD1[F]	PRD1[E]	PRD1[D]	PRD1[C]	PRD1[B]	PRD1[A]	PRD1[9]	PRD1[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X1A	Bank 1, R1A DT1L	Bit Name	DT1[7]	DT1[6]	DT1[5]	DT1[4]	DT1[3]	DT1[2]	DT1[1]	DT1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1B	Bank 1, R1B DT1H	Bit Name	DT1[F]	DT1[E]	DT1[D]	DT1[C]	DT1[B]	DT1[A]	DT1[9]	DT1[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X1C	Bank 1, R1C TMR1L	Bit Name	TMR1[7]	TMR1[6]	TMR1[5]	TMR1[4]	TMR1[3]	TMR1[2]	TMR1[1]	TMR1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1D	Bank 1, R1D TMR1H	Bit Name	TMR1[F]	TMR1[E]	TMR1[D]	TMR1[C]	TMR1[B]	TMR1[A]	TMR1[9]	TMR1[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X1E	Bank 1, R1E PWM2CR	Bit Name	PWM2E				T2EN	T2P2	T2P1	T2P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X1F	Bank 1, R1F PRD2L	Bit Name	PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X20	Bank 1, R20 PRD2H	Bit Name	PRD2[F]	PRD2[E]	PRD2[D]	PRD2[C]	PRD2[B]	PRD2[A]	PRD2[9]	PRD2[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X21	Bank 1, R21 DT2L	Bit Name	DT2[7]	DT2[6]	DT2[5]	DT2[4]	DT2[3]	DT2[2]	DT2[1]	DT2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X22	Bank 1, R22 DT2H	Bit Name	DT2[F]	DT2[E]	DT2[D]	DT2[C]	DT2[B]	DT2[A]	DT2[9]	DT2[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X23	Bank 1, R23 TMR2L	Bit Name	TMR2[7]	TMR2[6]	TMR2[5]	TMR2[4]	TMR2[3]	TMR2[2]	TMR2[1]	TMR2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X24	Bank 1, R24 TMR2H	Bit Name	TMR2[F]	TMR2[E]	TMR2[D]	TMR2[C]	TMR2[B]	TMR2[A]	TMR2[9]	TMR2[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X45	Bank 1, R45 TBPTL	Bit Name	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X46	Bank 1, R46 TBPTH	Bit Name	HLB	RDS	-	TB12	TB11	TB10	TB9	TB8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	0	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X47	Bank 1, R47 STKMON	Bit Name	STOF	-	-	-	-	STL2	STL1	STL0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	0	P	P	P
0X48	Bank 1, R48 PCH	Bit Name	-	-	-	PC12	PC11	PC10	PC9	PC8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	P	P	P	P	P
0X05	Bank 2, R5 TPEPCR 1	Bit Name	TPAEP 3	TPAEP 2	TPAEP 1	-	TPBEP 3	TPBEP 2	TPBEP 1	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X06	Bank 2, R6 TPEPCR 2	Bit Name	TPCEP 3	TPCEP 2	TPCEP 1	-	TPDEP 3	TPDEP 2	TPDEP 1	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X07	Bank 2, R7 TPEPCR 3	Bit Name	TPDE7	TPDE6	TPDE5	TPDE4	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	0
0X08	Bank 2, R8 TPCR1	Bit Name	-	-	-	TPICS	TPS	-	-	-
		Power-on	1	0	0	0	0	1	1	0
		/RESET and WDT	1	0	0	0	0	1	1	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X09	Bank 2, R9	Bit Name	-	-	-	-	-	-	-	-
		Power-on	1	1	0	0	0	0	0	0
		/RESET and WDT	1	1	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0A	Bank 2, RA TPDCR	Bit Name	TPDWO[7]	TPDWO[6]	TPDWO[5]	TPDWO[4]	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from	P	P	P	P	P	P	P	P

		Sleep/Idle								
0X0B	Bank 2, RB TPASCR	Bit Name	TPAEN	-	-	-	-	-	TPASW 1	TPASW 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0C	Bank 2, RC TPBSCR	Bit Name	TPBEN	-	-	-	-	-	TPBSW 1	TPBSW 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0D	Bank 2, RD TPCSCR	Bit Name	TPCEN	-	-	-	-	-	TPCSW 1	TPCSW 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0E	Bank 2, RE TPDSCR	Bit Name	TPDEN	-	-	-	-	-	TPDSW 1	TPDSW 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0F	Bank 2, RF	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X10	Bank 2, R10 GADCCR	Bit Name	-	-	-	GADCS 4	GADCS 3	GADCS 2	GADCS 1	-
		Power-on	0	0	0	1	0	1	0	0
		/RESET and WDT	0	0	0	1	0	1	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X11	Bank 2, R11 GBDCCR	Bit Name	-	-	-	GBDCS 4	GBDCS 3	GBDCS 2	GBDCS 1	-
		Power-on	0	0	0	1	0	1	0	0
		/RESET and WDT	0	0	0	1	0	1	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X12	Bank 2, R12 GCDCCR	Bit Name	-	-	-	GCDCS 4	GCDCS 3	GCDCS 2	GCDCS 1	-
		Power-on	0	0	0	1	0	1	0	0
		/RESET and WDT	0	0	0	1	0	1	0	0

		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X13	Bank 2, R13 GDDCCR	Bit Name	-	-	-	GDDCS4	GDDCS3	GDDCS2	GDDCS1	-
		Power-on	0	0	0	1	0	1	0	0
		/RESET and WDT	0	0	0	1	0	1	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X14	Bank 2, R14	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	1	0	1	0	0	0
		/RESET and WDT	0	0	1	0	1	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X15	Bank 2, R15	Bit Name	-	-	-	-	-	-	-	-
		Power-on	1	0	0	1	0	0	0	0
		/RESET and WDT	1	0	0	1	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X16	Bank 2, R16	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X17	Bank 2, R17	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	1	0	1	0
		/RESET and WDT	0	0	0	0	1	0	1	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X18	Bank 2, R18 TPSPCR	Bit Name	SPCY7	SPCY6	SPCY5	SPCY4	SPCY3	SPCY2	SPCY1	SPCY0
		Power-on	0	1	0	1	0	0	0	0
		/RESET and WDT	0	1	0	1	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X19	Bank 2, R19 TPAH	Bit Name	TPA[15]	TPA[14]	TPA[13]	TPA[12]	TPA[11]	TPA[10]	TPA[9]	TPA[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1A	Bank 2, R1A TPAL	Bit Name	TPA[7]	TPA[6]	TPA[5]	TPA[4]	TPA[3]	TPA[2]	TPA[1]	TPA[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1B	Bank 2,	Bit Name	TPB[15]	TPB[14]	TPB[13]	TPB[12]	TPB[11]	TPB[10]	TPB[9]	TPB[8]

	R1B TPBH	Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1C	Bank 2, R1C TPBL	Bit Name	TPB[7]	TPB[6]	TPB[5]	TPB[4]	TPB[3]	TPB[2]	TPB[1]	TPB[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1D	Bank 2, R1D TPCH	Bit Name	TPC[15]	TPC[14]	TPC[13]	TPC[12]	TPC[11]	TPC[10]	TPC[9]	TPC[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1E	Bank 2, R1E TPCL	Bit Name	TPC[7]	TPC[6]	TPC[5]	TPC[4]	TPC[3]	TPC[2]	TPC[1]	TPC[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1F	Bank 2, R1F TPDH	Bit Name	TPD[15]	TPD[14]	TPD[13]	TPD[12]	TPD[11]	TPD[10]	TPD[9]	TPD[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X20	Bank 2, R20 TPDL	Bit Name	TPD[7]	TPD[6]	TPD[5]	TPD[4]	TPD[3]	TPD[2]	TPD[1]	TPD[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X21	Bank 2, R21 DACR	Bit Name	-	-	-	-	-	-	DAE1	DAE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X22	Bank 2, R22 DACD0	Bit Name	DAD0[7]	DAD0[6]	DAD0[5]	DAD0[4]	DAD0[3]	DAD0[2]	DAD0[1]	DAD0[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X23	Bank 2, R23 DACD1	Bit Name	DAD1[7]	DAD1[6]	DAD1[5]	DAD1[4]	DAD1[3]	DAD1[2]	DAD1[1]	DAD1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from	P	P	P	P	P	P	P	P

		Sleep/Idle								

6.5 Interrupt

The eKTF5705 has 12 interrupts (External, Internal) as listed below:

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0	High 0
External	INT	ENI + EXIE=1	EXSF	2	1
External	Pin change	ENI +PxICIE=1	ICSF	4	2
Internal	TCC	ENI + TCIE=1	TCSF	6	3
Internal	SPI	ENI + SPIIE=1	SPISF	C	4
Internal	PWMP1	ENI+PWM1PIE=1	PWM1PSF	14	6
Internal	PWMD1	ENI+PWM1DIE=1	PWM1DSF	16	7
Internal	I^2C Transmit	ENI+ I2CTIE	I2CTSF	1A	8
Internal	I^2C Receive	ENI+ I2CRIE	I2CRSF	1C	9
Internal	I2CSTOP	ENI+ I2CSTPIE	I2CSTPSF	1E	10
Internal	PWMP2	ENI+PWM2PIE=1	PWM2PSF	24	11
Internal	PWMD2	ENI+PWM2DIE=1	PWM2DSF	26	12

Bank 0 R14~R19 are the interrupt status registers that record the interrupt requests in the relative flags/bits. Bank0 R1B~R20 are the interrupt Mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICSF bit delete) in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

External interrupt is equipped with digital noise rejection circuit (input pulse of less than **4 system clock time** is eliminated as noise). When an interrupt (Falling edge) is generated by the External interrupt (if enabled), the next instruction will be fetched from Address 002H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 (Bit 0~Bit 4) and R4 registers are saved by hardware. If another interrupt occurs, the ACC, R3 (Bit 0~Bit 4), and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, ACC, R3 (Bit0~Bit4), and R4 restored.

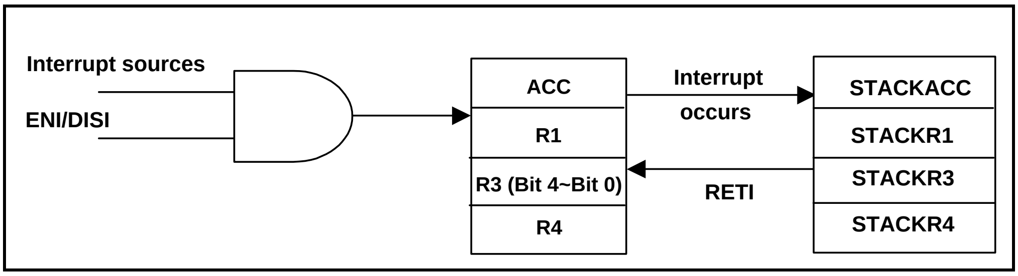


Figure 6-6a Interrupt Backup Diagram

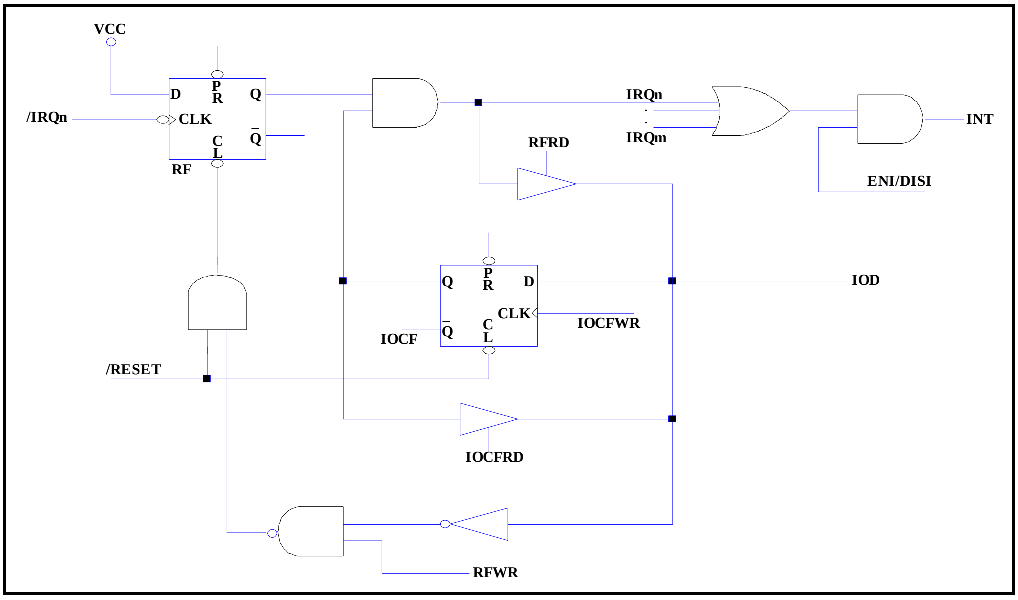


Figure 6-6b Interrupt Input Circuit

6.6 Dual Set of PWM (Pulse Width Modulation)

6.6.1 *Overview*

In PWM mode, PWM1 and PWM2 produce up to 16-bit resolution PWM output (see. functional block diagram below). A PWM output consists of a time period and a duty cycle, and it keeps the output high. The PWM baud rate is the inverse of the time period. Figure 6-7b below; *PWM Output Timing*, depicts the relationships between a time period and a duty cycle.

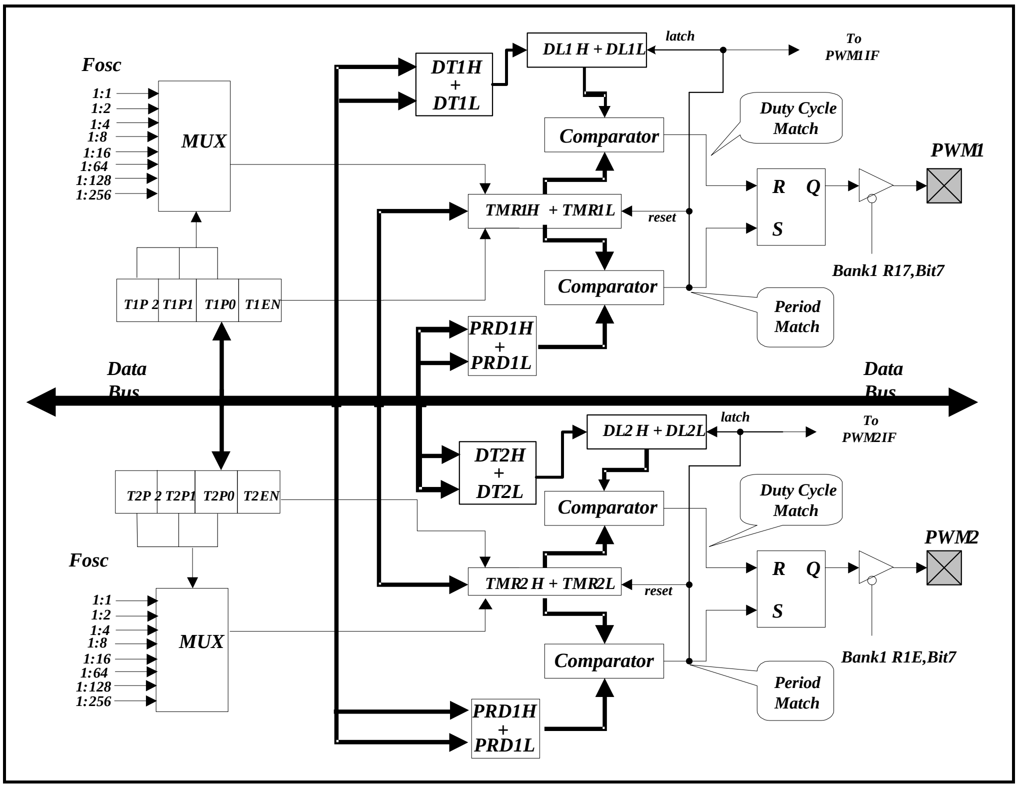


Figure 6-7a Dual PWMs Functional Block Diagram

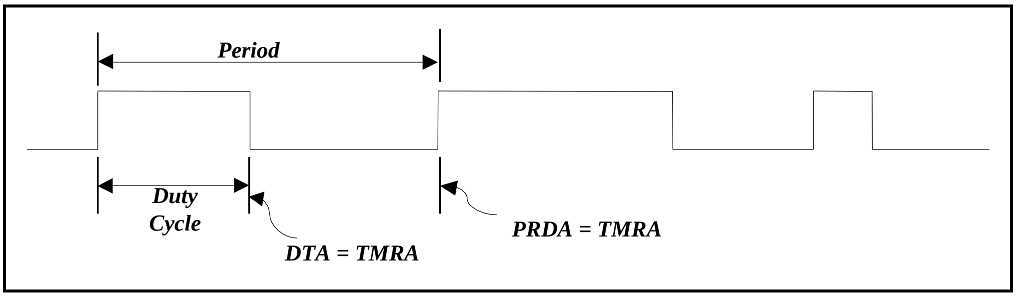


Figure 6-7b PWM Output Timing

6.6.2 Control Register

R_BANK	Addres	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x17	SFR3	-	-	-	-	PWM2PSF	PWM2DS_	PWM1PSF	PWM1DS_
			-	-	-	-	F	F	F	F
Bank 0	0x1D	IMR3	-	-	-	-	PWM2PIE	PWM2DIE	PWM1PIE	PWM1DIE
			-	-	-	-	R/W	R/W	R/W	R/W
Bank 1	0x16	PWMSCR	-	-	-	-	-	-	PWM2S	PWM1S
			-	-	-	-	-	-	R/W	R/W
Bank 1	0x17	PWM1CR	PWM1E	-	-	-	T1EN	T1P2	T1P1	T1P0
			R/W	-	-	-	R/W	R/W	R/W	R/W
Bank 1	0x18	PRD1L	PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x19	PRD1H	PRD1[F]	PRD1[E]	PRD1[D]	PRD1[C]	PRD1[B]	PRD1[A]	PRD1[9]	PRD1[8]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1A	DT1L	DT1[7]	DT1[6]	DT1[5]	DT1[4]	DT1[3]	DT1[2]	DT1[1]	DT1[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1B	DT1H	DT1[F]	DT1[E]	DT1[D]	DT1[C]	DT1[B]	DT1[A]	DT1[9]	DT1[8]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1C	TMR1L	TMR1[7]	TMR1[6]	TMR1[5]	TMR1[4]	TMR1[3]	TMR1[2]	TMR1[1]	TMR1[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1D	TMR1H	TMR1[F]	TMR1[E]	TMR1[D	TMR1[C	TMR1[B]	TMR1[A]	TMR1[9]	TMR1[8]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1E	PWM2CR	-	-	-	-	T2EN	T2P2	T2P1	T2P0
			-	-	-	-	R/W	R/W	R/W	R/W
Bank 1	0x1F	PRD2L	PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x20	PRD2H	PRD2[F]	PRD2[E]	PRD2[D]	PRD2[C]	PRD2[B]	PRD2[A]	PRD2[9]	PRD2[8]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x21	DT2L	DT2[7]	DT2[6]	DT2[5]	DT2[4]	DT2[3]	DT2[2]	DT2[1]	DT2[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x22	DT2H	DT2[F]	DT2[E]	DT2[D]	DT2[C]	DT2[B]	DT2[A]	DT2[9]	DT2[8]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x23	TMR2L	TMR2[7]	TMR2[6]	TMR2[5]	TMR2[4]	TMR2[3]	TMR2[2]	TMR2[1]	TMR2[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x24	TMR2H	TMR2[F]	TMR2[E]	TMR2[D	TMR2[C	TMR2[B]	TMR2[A]	TMR2[9]	TMR2[8]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.6.3 Increment Timer Counter (TMRX: TMR1H/TMR1L, TMR2H/TMR2L)

TMRX's are 16-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMR can be read only. If employed, they can be turned off for power saving by setting the T1EN bit [BANK1-R17 <3>], T2EN bit [BANK1-R1E<3>] to "**0**". TMR1and TMR2, are internal designs and cannot be read.

6.6.4 PWM Time Period (PRDX: PRD1L/H, PRD1L/H)

The PWM time period is 16-bit resolution and is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

1) TMRX is cleared
2) The PWMX pin is set to "**1**"

> **NOTE**
> *The PWM output cannot be set if the duty cycle is "**0**."*

3) The PWMXPSF bit is set to "**1**"

To calculate the PWM time period, use the following formula**:**

$$Period = (PRDX + 1) \times \left(\frac{1}{F_{OSC}}\right) \times (TMRX\ \ prescale\ \ value)$$

Example:

PRDX = 49; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 1;

Then –

$$Period = (49 + 1) \times \left(\frac{1}{4M}\right) \times 1 = 12.5\mu s$$

6.6.5 PWM Duty Cycle (DTX: DT1H/DT1L, DT2H/DT2L)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded anytime. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula shows how to calculate the PWM duty cycle:

$$Duty\ cycle = (DTX) \times \left(\frac{1}{F_{OSC}}\right) \times (TMRX\ \ prescale\ value)$$

Example:

DTX = 10; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 1;

Then –

$$Duty\ cycle = (10) \times \left(\frac{1}{4M}\right) \times 1 = 2.5\mu s$$

6.6.6 PWM Programming Process/Steps

1) Load the PWM duty cycle to DT
2) Load the PWM time period to PRD
3) Enable the interrupt function by writing Bank0-R1D, if required
4) Load a desired value for the timer prescaler
5) Enable PWMX function, i.e., enable PWMXE control bit
6) Finally, enable TMRX function, i.e., enable TXEN control bit

If the application needs to change PWM duty and period cycle at run time, refer to the following programming steps:

1) Load new duty cycle (if using dual PWM function) at any time.
2) Load new period cycle. You must take note of the order of loading period cycle. As the low byte of PWM period cycle is assigned a value, the new PWM cycle is loaded into circuit.
3) The circuit will automatically update the new duty and period cycles to generate new PWM waveform at the next PWM cycle.

6.7 SPI (Serial Peripheral Interface)

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0X36	SPICR	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
			R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Bank 0	0X37	SPIS	DORD	TD1	TD0	-	OD3	OD4	-	RBF
			R/W	R/W	R	-	R/W	R/W	-	R/W
Bank 0	0X38	SPIR	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
			R	R	R	R	R	R	R	R
Bank 0	0X39	SPIW	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X18	SFR4	-	-	-	-	SPSF	-	-	-
			-	-	-	-	R/W	-	-	-
Bank 0	0X1E	IMR4	-	-	-	-	SPIE	-	-	-
			-	-	-	-	R/W	-	-	-

6.7.1 Overview and Features

■ **Overview:**

Figures 6-8a and 6-8b below show how the eKTF5705 communicates with other devices through SPI module. If the eKTF5705 is the Master controller, it will send clock through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if the eKTF85705 is defined as a Slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both clock rate and the selected edge. User can also set the –

- SPIS Bit 7(DORD) to determine the SPI transmission order,
- SPICR Bit 3 (SDOC) to control SDO pin after serial data output status,
- SPIS Bit 6 (TD1) and Bit 5 (TD0) determine the SDO status output delay times.

■ **Features:**

1) Operation in either Master mode or Slave mode
2) Three-wire or four-wire full duplex synchronous communication
3) Programmable baud rates of communication
4) Programmable clock polarity, (Bank 0 R36 Bit7)
5) Interrupt flag available for read buffer full
6) SPI transmission order
7) SDO status select after serial data output
8) SDO status output delay time
9) SPI handshake pin
10) Up to 8 MHz (maximum) bit frequency

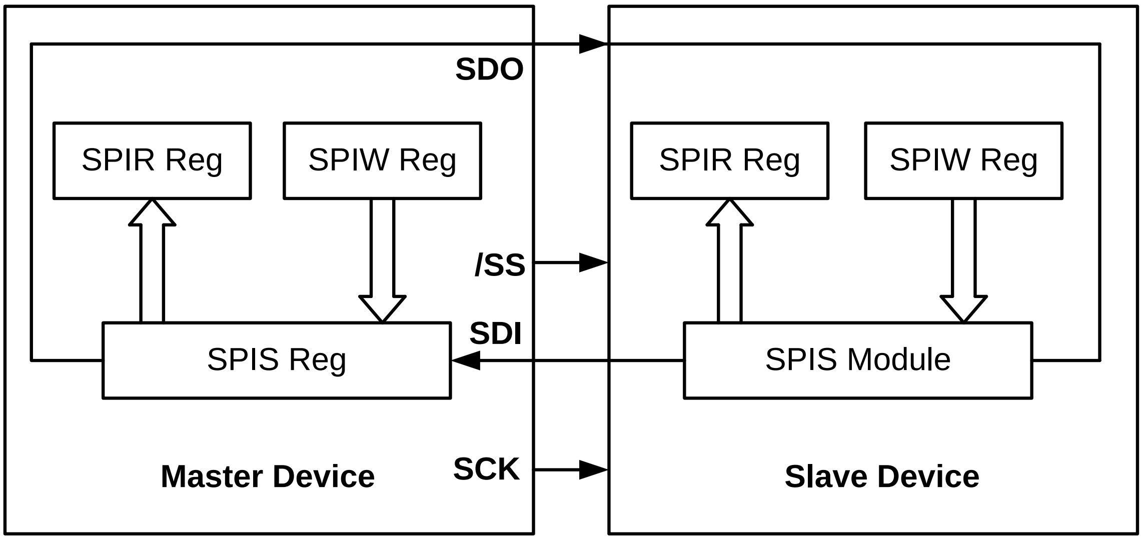


Figure 6-8a SPI Master/Slave Communication Block Diagram

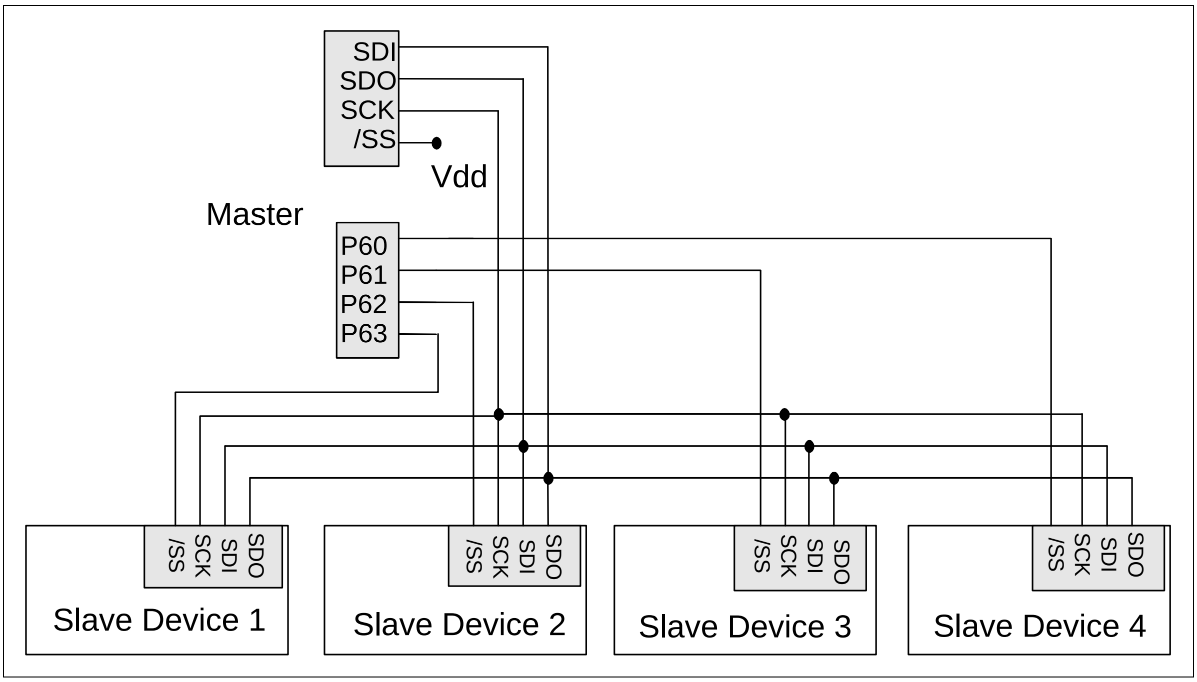


Figure 6-8b Single-Master and Multi-Slave SPI Configuration

6.7.2 SPI Function Description

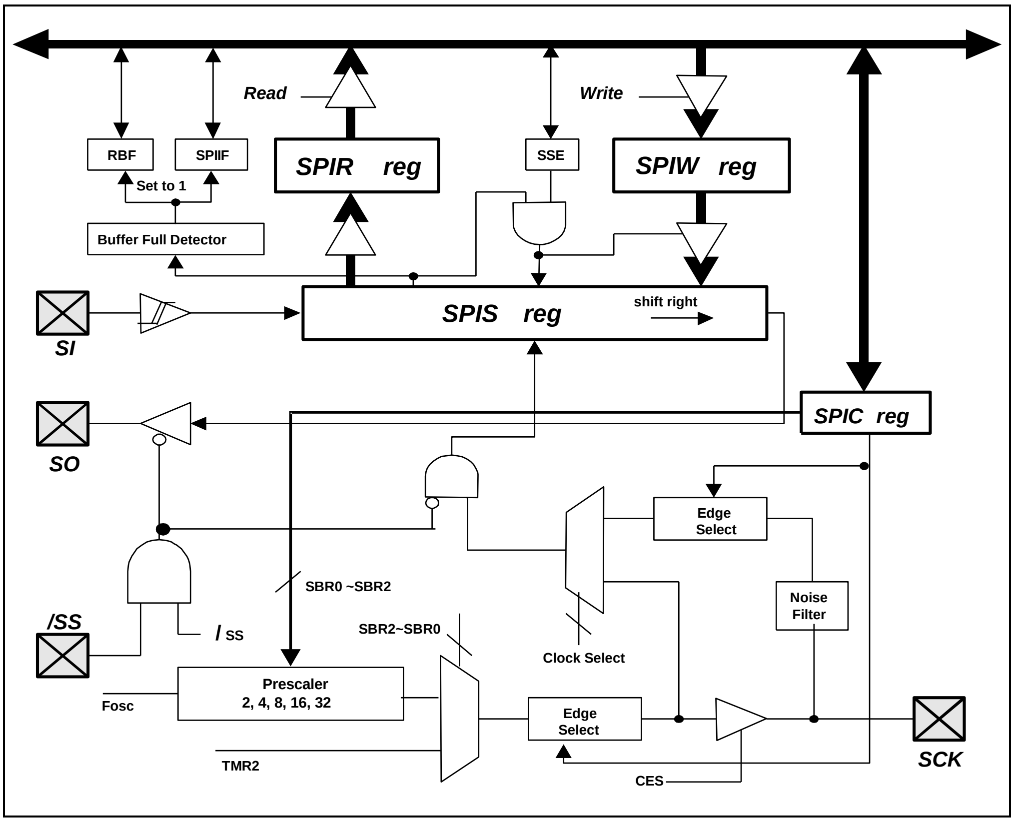


Figure 6-9a SPI Function Block Diagram

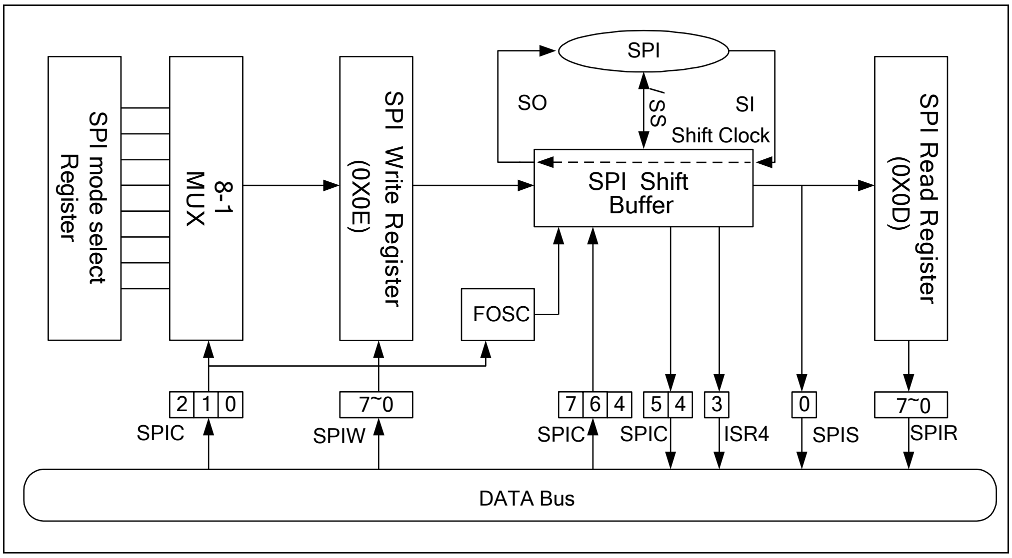


Figure 6-9b SPI Transmission Function Block Diagram

The following explains the functions of each block in the above figures as SPI carries out communication with the depicted signals**:**

- **P52/SI/TPA2:** Serial Data In
- **P51/SO/TPA1:** Serial Data Out
- **P53/SCK/TPA3:** Serial Clock
- **P50//SS/TPA0:** /Slave Select (Option). This pin (/SS) may be required during Slave mode
- **RBF:** Set by Buffer Full Detector
- **Buffer Full Detector:** Set to 1 when an 8-bit shifting is completed.
- **SSE:** Loads the data in SPIS register, and begin to shift. The SSE bit will be kept in "**1**" if the communication is still undergoing. This flag must be cleared as shifting is completed. You can determine if the next write attempt is available.
- **SPIS reg.:** Shifting byte in and out. The MSB is shifted first. Both the SPIR and the SPIW registers are shifted at the same time. Once data are written, SPIS starts transmitting / receiving. The data received will be moved to the SPIR register as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the SPISF (SPI Interrupt) flag are then set.
- **SPIR reg.:** Read buffer. The buffer is updated as the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPIR register reads.
- **SPIW reg.:** Write buffer. The buffer will deny any attempts to write until the 8-bit shifting is completed.
- **SBRS2~SBRS0:** Programming of the clock frequency/rates and sources.
- **Clock Select:** Select either the internal or the external clock as shifting clock.
- **Edge Select:** Select the appropriate clock edges by programming the CES bit

6.7.3 SPI Signal and Pin Description

The detailed functions of the four pins, SI, SO, SCK, and /SS are as follows**:**

- **P52/SI/TPA2:**

- Serial Data In
- Receive sequentially, the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
- Defined as high-impedance, if not selected.

- Program the same clock rate and clock edge to latch on both the Master and Slave devices.
- The byte received will update the transmitted byte.
- The RBF will be set as the SPI operation is completed.
- Timing is shown in Figures 6-10a and 6-10b below.

■ **P51/SO/TPA1:**

- Serial Data Out
- Transmit sequentially; the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
- Program the same clock rate and clock edge to latch on both the Master and Slave devices.
- The received byte will update the transmitted byte.
- The CES bit is reset, as the SPI operation is completed.
- Timing is shown in Figures 6-10a and 6-10b.

■ **P53/SCK/TPA3:**

- Serial Clock
- Generated by a Master device
- Synchronize the data communication on both the SI and SO pins.
- The CES is used to select the edge to communicate.
- The SBR0~SBR2 is used to determine the baud rate of communication.
- The CES, SBR0, SBR1, and SBR2 bits have no effect in Slave mode.
- Timing is shown in Figures 6-10a and 6-10b.

■ **P50//SS/TPA0:**

- Slave Select; negative logic.
- Generated by a Master device to indicate the Slave(s) has to receive data.
- Goes low before the first cycle of SCK occurs, and remains low until the last (8th) cycle is completed
- Ignore the data on the SI and SO pins when /SS is high, because the SO is no longer driven
- Timing is shown in Figures 6-10a and 6-10b.

6.7.4 SPI Mode Timing

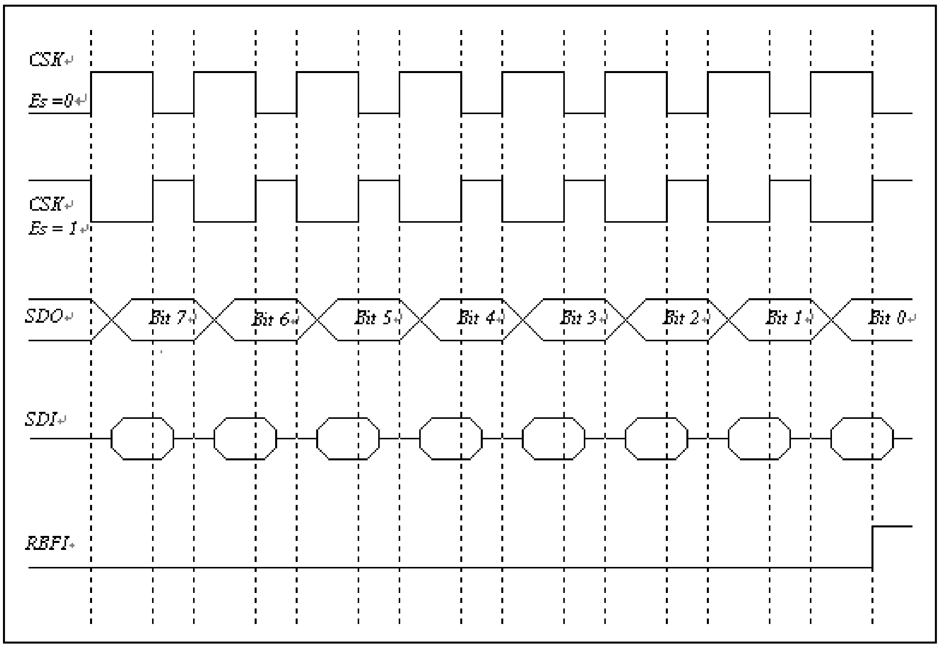


Figure 6-10a SPI Mode with /SS Disabled Timing Diagram

The SCK edge is selected by programming the bit CES. The waveform shown in Figure 6-10a above, is applicable regardless of whether the eKTF5705 is in Master or Slave mode with /SS disabled. However, the waveform in Figure 6-10b below can only be implemented in Slave mode with /SS enabled.

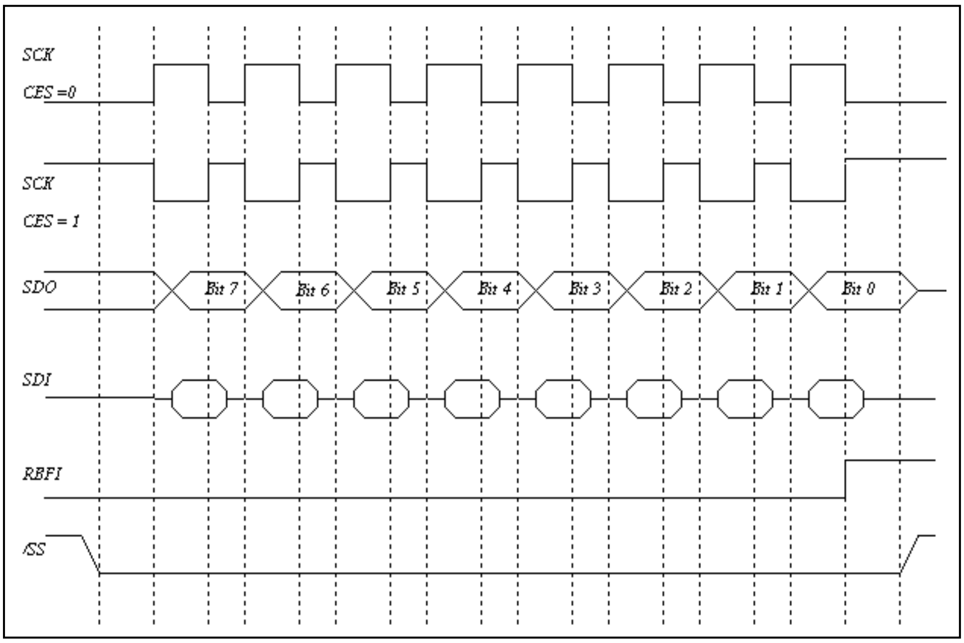


Figure 6-10b SPI Mode with /SS Enabled Timing Diagram

6.8 I²C Function

The I²C function and transmit/receive pin are enabled by default when eKTF5705 is powered-on.

■ **Registers for I²C circuit:**

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x30	I2CCR1	Strobe /Pend	IMS	ISS	STOP	SAR_ EMPTY	ACK	FULL	EMPTY
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x31	I2CCR2	I2CBF	GCEN	-	BBF	I2CTS1	I2CTS0	-	I2CEN
			R	R/W	-	R	R/W	R/W	-	R/W
Bank 0	0x32	I2CSA	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x33	I2CDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x34	I2CDAL	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x35	I2CDAH	-	-	-	-	-	-	DA9	DA8
			-	-	-	-	-	-	R/W	R/W
Bank 0	0x18	SFR4	-	-	-	-	-	I2CSTPIF	I2CRSF	I2CTSF
			-	-	-	-	-	R/W	R/W	R/W
Bank 0	0x1E	IMR4	-	-	-	-	-	I2CSTPIE	I2CRIE	I2CTIE
			-	-	-	-	-	R/W	R/W	R/W

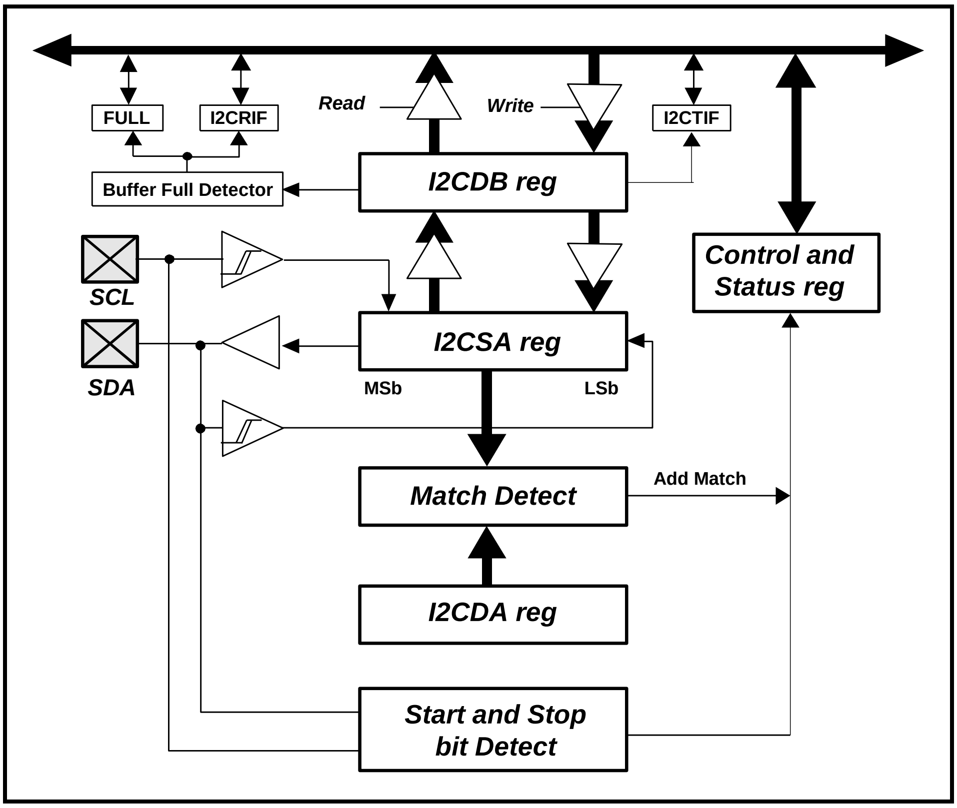


Figure 6-11 eKTF5705 I^2C Block Diagram

The eKTF5705 supports a bidirectional, 2-wire bus, 7/10-bit addressing, and data transmission protocol. A device that sends data to the bus is defined as transmitter, while a device receiving the data is defined as a receiver. The bus has to be controlled by a Master device which generates the Serial Clock (SCL), controls the bus access, and generates the Start and Stop conditions. Both Master and Slave can operate as transmitter or receiver, but the Master device determines which mode is activated.

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. The output stages of the devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I^2C-bus can be transferred at the rates of up to 100 kbit/s in Standard-mode or up to 400 kbit/s in Fast-mode.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW.

The I^2C interrupt occurs as describe below:

Condition	Master/Slave	Transmit Address	Transmit Data	Stop
Master Transmitter (transmits to Slave-Receiver)	Master	Transmit interrupt	Transmit interrupt	Stop interrupt
	Slave	Receive interrupt	Receive interrupt	Stop interrupt
Master Receiver (read Slave-Transmitter)	Master	Transmit interrupt	Receive interrupt	Stop interrupt
	Slave	Transmit interrupt	Transmit interrupt	Stop interrupt

Within the procedure of the I^2C bus, unique situations could arise which are defined as START (S) and STOP (P) conditions.

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

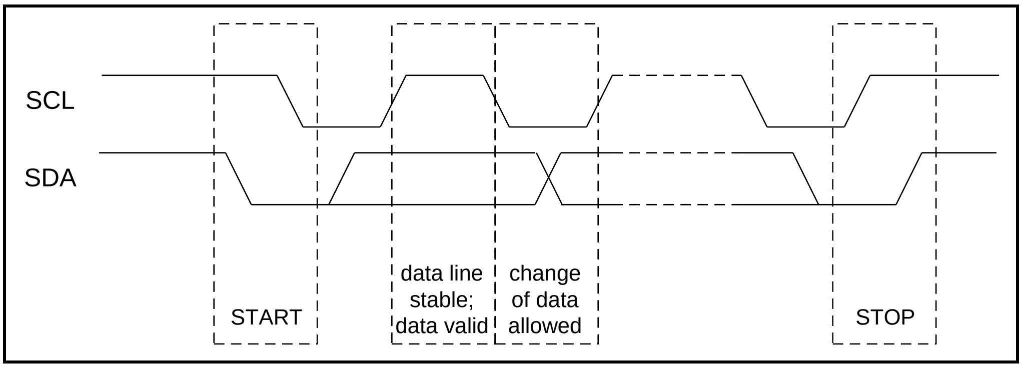


Figure 6-12 I^2C Transfer Condition

6.8.1 7-Bit Slave Address

Master-transmitter transmits to Slave-receiver. The transfer direction is not changed.

Master reads Slave immediately after first byte. At the moment of the first acknowledgement, the Master-transmitter becomes a Master-receiver and the Slave-receiver becomes a Slave-transmitter. This first acknowledgement is still generated by the Slave. The STOP condition is generated by the Master, which has previously sent a Not-Acknowledge (A). The difference between Master-transmitter and Master-receiver is only in their R//W bit. If the R//W bit is "**0**", the Master device would be transmitter. Otherwise, the Master device would be the receiver (R//W bit="**1**").

Communications between the Master-transmitter/receiver and Slave-transmitter/receiver are illustrated in the following Figures 6-13a and 6-13b.

NOTE
Slave Address 0x77 is reserved for WTR use.

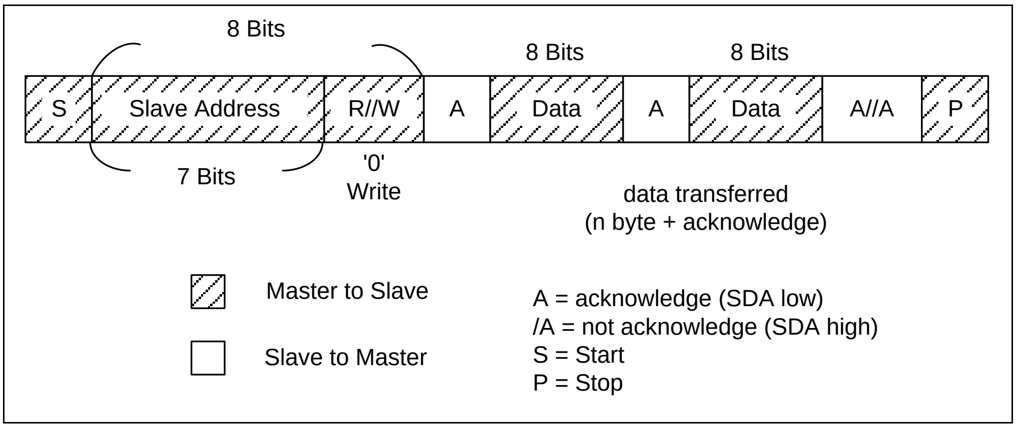


Figure 6-13a Master-Transmitter Transmits to Slave-Receiver with 7-Bit Slave Address

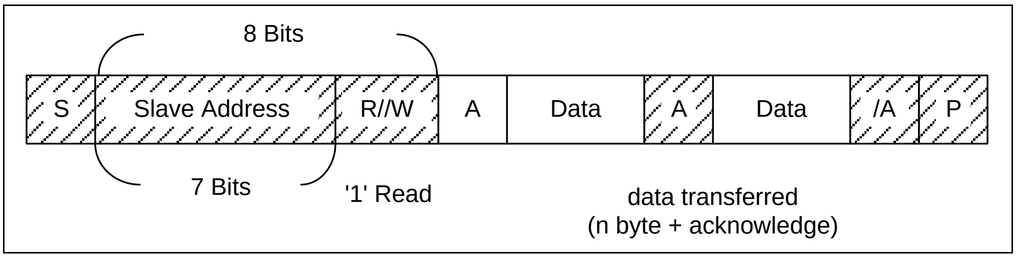


Figure 6-13b Master-Receiver Reads from Slave-Transmitter with 7-Bit Slave Address

6.8.2 10-Bit Slave Address

In 10-Bit Slave address mode, using 10-bit for addressing exploits the reserved combination 11110XX for the first seven bits of the first byte following a START(S) or repeated START (Sr) condition. The first seven bits of the first byte are the combination 11110XX of which the last two bits (XX) are the two most-significant bits of the 10-bit address. If the R/W bit is “**0**”, the second byte after acknowledge would be the eight address bits of 10-bits Slave address. Otherwise, the second byte would just be the next transmitted data from a Slave to Master device. The first byte 11110XX is transmitted by using the Slave address register (I2CSA), and the second byte XXXXXXXX is transmitted by using the data buffer (I2CDB).

The possible data transfer formats for 10-bit Slave address mode are explained in the following paragraphs and Figures 6-14a ~ 6-14e.

■ Master-Transmitter Transmits to Slave-Receiver with a 10-bit Slave Address

When the Slave receives the first byte after START bit from Master, each Slave device will compare the first seven bits of the first byte (11110XX) with their own address and check the 8th bit (R/W). If the R/W bit is "**0**", a Slave or more, will return an Acknowledge (A1). Then all Slave devices will continue to compare the second address (XXXXXXXX). If a Slave device finds a match, that particular Slave device will be the only one to return an Acknowledge (A2). The matched Slave device will remain addressed by the Master until it receives the STOP condition or until a repeated START condition followed by the different Slave address is received.

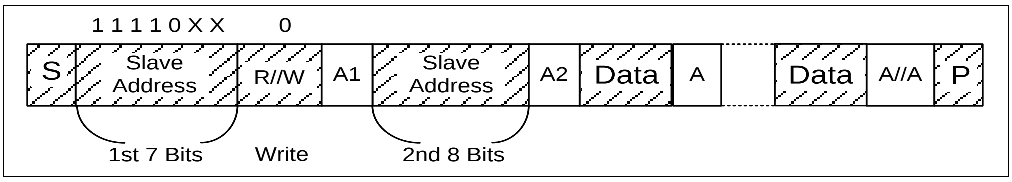


Figure 6-14a Master-Transmitter Transmits to Slave-Receiver with a 10-Bit Slave Address

■ Master-Receiver Read Slave-Transmitter with a 10-bit Slave Address

Up to, and including Acknowledge Bit A2, the procedure is the same as that described above for Master-Transmitter addressing a Slave-Receiver. After the Acknowledge (A2), a repeated START condition (Sr) takes place followed by seven bits Slave address (11110XX), but the 8th bit R/W is "**1**." The addressed Slave device will then return the Acknowledge (A3). If the repeated START (Sr) condition occurs and the seven bits of first byte (11110XX) are received by Slave device, all the Slave devices will compare with their own address and check the 8th bit (R/W). However, none of the Slave devices can return an acknowledgement because R/W=1.

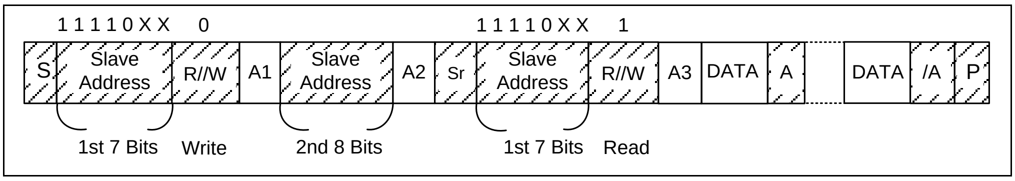


Figure 6-14b Master-Receiver reads Slave-Transmitter with a 10-Bit Slave Address

■ Master Transmits and Receives Data to and from the Same Slave Device with 10-Bit Addresses

The initial operation of this data transfer format is the same as explained in the above paragraph on "*Master-Transmitter transmits to Slave-Receiver with a 10-bit Slave Address.*" Then the Master device starts to transmit the data to Slave device. When the Slave device receives the Acknowledge or None-Acknowledge that is followed by repeat START (Sr), the above operation under "*Master-Receiver Read Slave-Transmitter with a 10-Bit Slave Address*" is repeatedly performed.

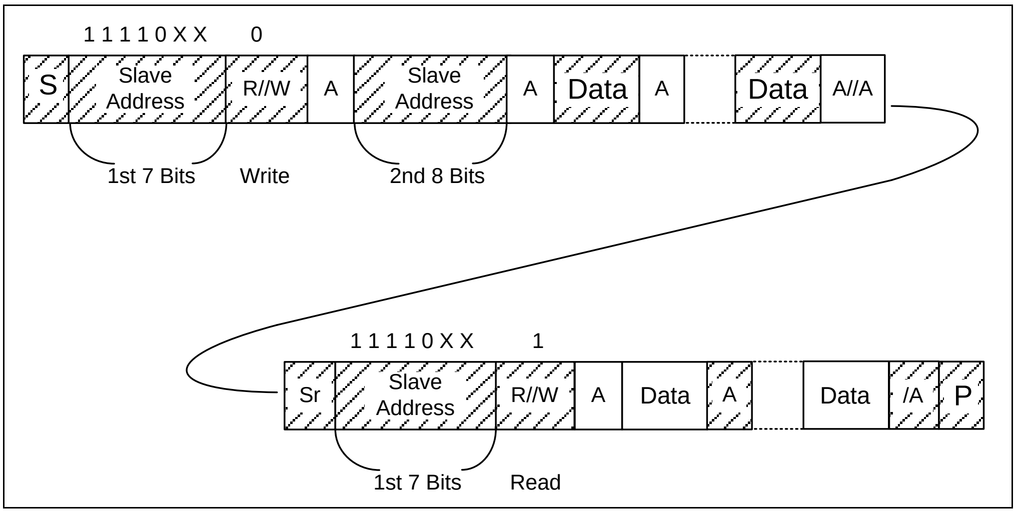


Figure 6-14c Master Addresses a Slave with 10-Bit Addresses Transmits and Receives Data with the Same Slave Device

■ Master Device Transmits Data to Two or More Slave Devices with 10 & 7 Bits Slave Address

For 10-bit address, the initial operation of this data transfer format is the same as explained in the above paragraph on "*Master-Transmitter transmits to Slave-Receiver with a 10-bit Slave Address,*" which describes how to transmit data to Slave device. After the Master device completes the initial transmittal, and wants to continue transmitting data to another device, the Master needs to address each of the new Slave devices by repeating the initial operation mentioned above. If the Master device wants to transmit the data in 7-bit and 10-bit Slave address modes successively, this could be done after the Start or repeat Start conditions as illustrated in the following figures.

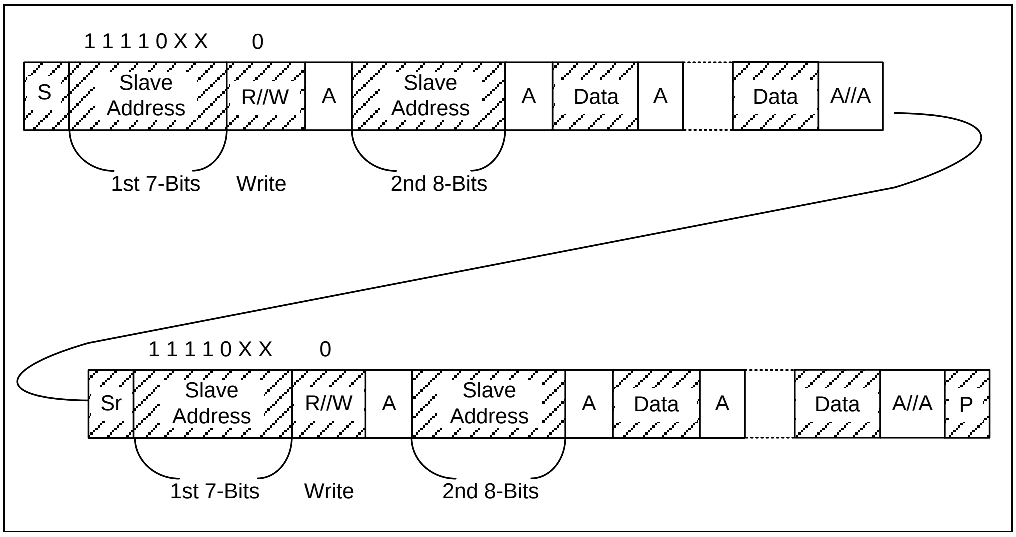


Figure 6-14d Master Transmitting to More than One Slave Devices with 10-Bit Slave Address

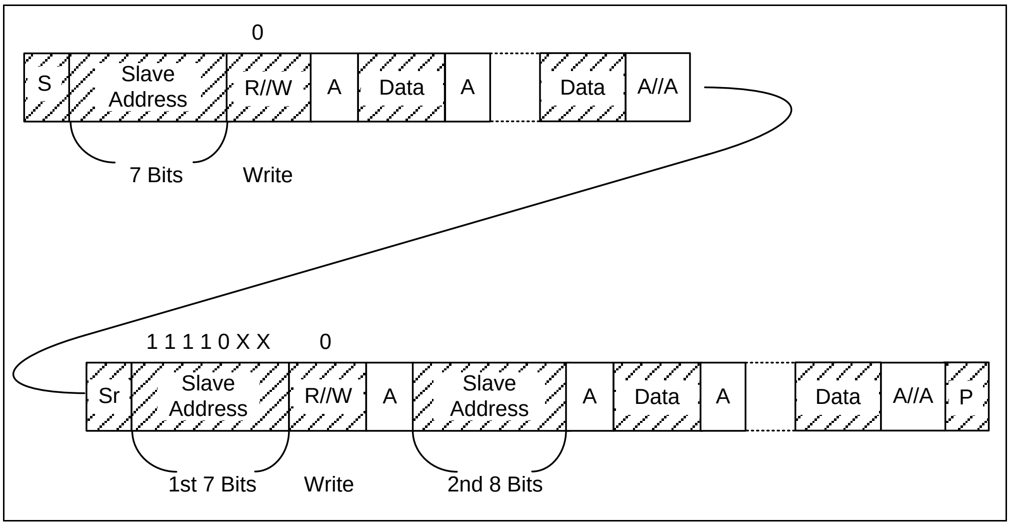


Figure 6-14e Master Successively Transmitting to 7-Bit and 10-Bit Slave Address

6.8.3 Master Mode

In transmitting (receiving) serial data, the I^2C is carried on as follows:

1) Set I2CTS1~0, I2CCS, and ISS bits to select I^2C transmit clock source.
2) Set I2CEN and IMS bits to enable I^2C Master function.
3) Write Slave address into the I2CSA register and IRW bit to select read or write.
4) Set strobe bit to start transmitting and then check I2CTSF (I2CTSF) bit.
5) Write 1^{st} data into the I2CDB register, set strobe bit, and check I2CTSF (I2CRSF) bit.
6) Write 2^{nd} data into the I2CDB register, set strobe bit, STOP bit, and check I2CTSF (I2CRSF) bit.

6.8.4 Slave Mode I^2C Transmit

In receiving (transmitting) serial data, the I^2C is carried on as follows:

1) Set I2CTS1~0, I2CCS, and ISS bits to select I^2C transmit clock source.
2) Set I2CEN and IMS bits to enable I^2C Slave function.
3) Write device address into the I2CDA register.
4) Check I2CRSF (I2CTSF) bit, read I2CDB register (address), and then clear the Pend bit.
5) Check I2CRSF (I2CTSF) bit, read I2CDB register (1st data), and then clear the Pend bit.
6) Check I2CRSF (I2CTSF) bit, read I2CDB register (2nd data), and then clear the Pend bit.
7) Check the I2CSTPSF bit, end transmission.

6.9 Oscillator

6.9.1 Oscillator Modes

The eKTF5705 can be operated in the one oscillator mode, i.e., Internal RC oscillator mode (IRC). You need to set the main-oscillator modes by selecting the OSC0, and set sub-oscillator modes by selecting the FSS in the Code Option register to complete the overall oscillator mode setting.

■ **Main-Oscillator Modes Defined By OSC0**

Main-Oscillator Mode	OSC0
IRC (Internal RC oscillator mode; default) RCOUT (P54) acts as I/O pin	1
IRC (Internal RC oscillator mode) RCOUT (P54) acts as clock output pin	0

■ **Summary of Maximum Operating Speeds**

Conditions	VDD	Fxt Max. (MHz)
Two cycles with two clocks	2.5	4.0
	2.5	8.0
	2.5	12.0
	2.5	16.0

6.9.2 Internal RC Oscillator Mode

The eKTF5705 offers a versatile internal RC mode with default frequency value of 4 MHz. The Internal RC oscillator mode has other frequencies (16 MHz, 8 MHz, and 12 MHz) that can be set by Code Option; RCM1 and RCM0. The Table below describes a typical drift rate of the calibration.

■ **Internal RC Drift Rate (Ta=25°C, VDD=3.6V±5%, VSS=0V)**

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~+85°C)	Voltage (2.5V~3.6V)	Process	Total
12 MHz	± 2%	± 1%	± 1%	± 4%
4 MHz	± 2%	± 1%	± 1%	± 4%
8 MHz	± 2%	± 1%	± 1%	± 4%
16 MHz	± 2%	± 1%	± 1%	± 4%

Note: *These are theoretical values intended for reference only. Actual values may vary depending on actual conditions.*

6.10 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply reaches its steady state. The eKTF5705 is equipped with a Power-on Voltage Detector (POVD) with a detection level of 2.2V. It will work well if Vdd rises fast enough (50 ms or less). However, in critical applications, extra devices are still required to assist in solving power-up problems.

6.11 External Power-on Reset Circuit

The circuits diagram in Figure 6-15 implements an external RC to generate the reset pulse. The pulse width (time constant) should be kept long enough for VDD to reach minimum operational voltage. Apply this circuit when the power supply has slow rise time. Since the current leakage from the /RESET pin is about ± 5 µA, it is recommended that R should not be greater than 40KΩ in order for the /RESET pin voltage to remain at below 0.2V. The diode (D) functions as a short circuit at the instant of power down. The capacitor (C) will discharge rapidly and fully. The current-limited resistor (Rin) will prevent high current or ESD (electrostatic discharge) from flowing into /RESET pin.

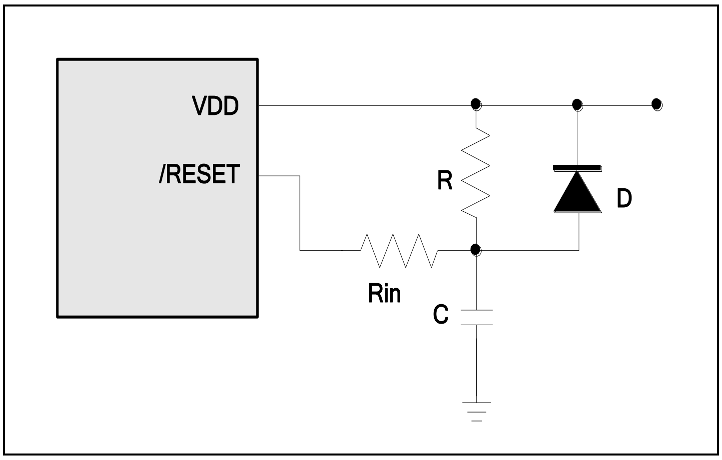


Figure 6-15 External Power-Up Reset Circuit

6.12 Residue-Voltage Protection

When the battery is replaced, device power (VDD) is taken off but residue-voltage remains. The residue-voltage may trips below VDD minimum, but not to zero. This condition may cause a poor power-on reset. Figures 6-16a and 6-16b show how to accomplish a proper residue-voltage protection circuit.

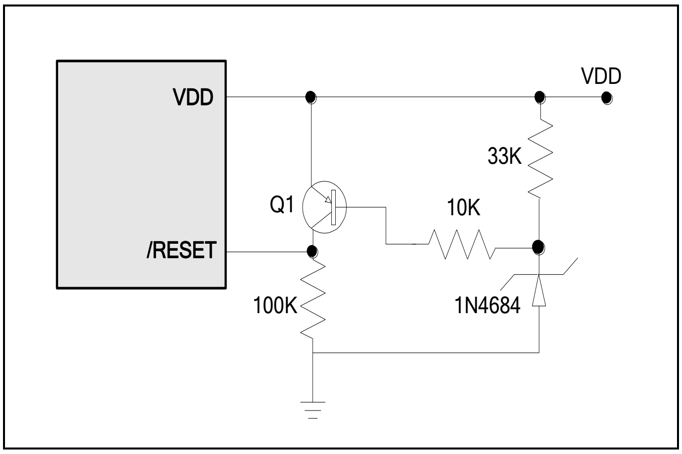


Figure 6-16a Circuit 1 for Residue Voltage Protection

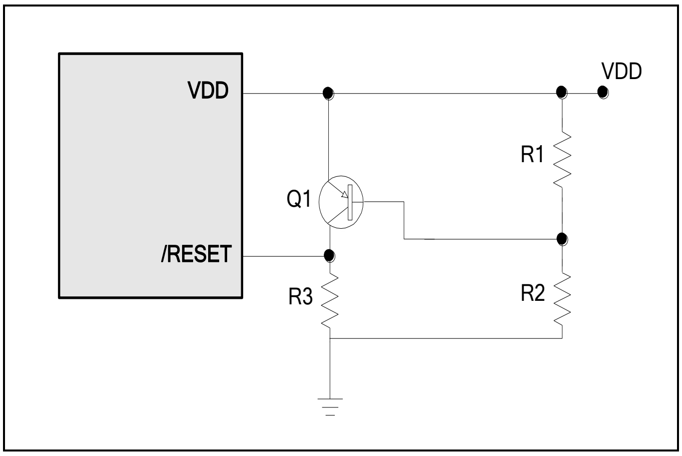


Figure 6-16b Circuit 2 for Residue Voltage Protection

6.13 Code Option

6.13.1 Code Option Register (Word 0)

Word 0															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**-**	**IRCWUT**	**-**	**-**	**HLFS**	**-**	**LVR1**	**LVR0**	**RESETEN**	**ENWDT**	**NRHL**	**NRE**	**PR2**	**PR1**	**PR0**
1	High	8 clks	High	High	Normal	High	High	High	P57	Disable	32/fc	Enable	Disable		
0	Low	32 clks	Low	Low	Green	Low	Low	Low	/RST	Enable	8/fc	Disable	Enable		
Default	1	1	1	1	1	1	1	1	1	1	1	1	1		

Bits 14: Not used. Set to "**1**" all the time.

Bit 13 (IRCWUT): IRC Warm-up Time (back to Normal mode)

0: 32 clocks

1: 8 clocks (default)

Bits 12~11: Not used. Set to "**1**" all the time.

Bit 10 (HLFS): Reset to Normal or Green Mode select bit

0: CPU is selected to enter into Green mode when a reset occurs.

1: CPU is selected to enter into Normal mode when a reset occurs (default).

Bit 9: Not used. Set to "**1**" all the time.

Bits 8~7 (LVR1~LVR0): Low Voltage Reset enable bit

LVR1, LVR0	VDD Reset Level	VDD Release Level
1x	NA (Power-on reset; default)	
01	2.7V *	2.9V
00	3.0V **	3.2V

* *If VDD < 2.7V and is kept for about 5 μs, IC will reset.*

** *If VDD < 3.0V and is kept for about 5 μs, IC will reset.*

Bit 6 (RESETEN): P80//RESET pin select bit

0: Enable /RESET pin

1: Disable P80 pin (default)

Bit 5 (ENWDT): WDT Enable bit

0: Enable

1: Disable (default)

Bit 4 (NRHL): Noise Rejection High/Low pulse definition bit

0: Pulses equal to 8/fc [s] is considered as valid signal

1: Pulses equal to 32/fc [s] is considered as valid signal (default)

Bit 3 (NRE): Noise Rejection Enable bit

0: Disable

1: Enable (default)

NOTE

During Green, Idle, and Sleep modes, the Noise Rejection circuit is always disabled.

Bits 2~0 (PR2 ~ PR0): Protect bit. Each protect status is as follows:

PR2	PR1	PR0	Protect
0	0	0	Enable
1	1	1	Disable

6.13.2 Code Option Register (Word 1)

Word 1															
Bit	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	FSS	C5	C4	C3	C2	C1	C0	RCM1	RCM0	DAS	-	-	OSC0	RCOUT
1	-	High	High	High	High	High	High	High	High	High	0x77	-	-	High	High
0	-	Low	Low	Low	Low	Low	Low	Low	Low	Low	User	-	-	Low	Low
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit 14: Not used. Set to "**1**" all the time.

Bits 13 (FSS): Sub-oscillator mode select bit

0: Fs is 64kHz

1: Fs is 16kHz

NOTE

WDT frequency is always 16kHz regardless of the FSS[1:0] bits setting.

Bits 12~7 (C5~C0): IRC trim bits (auto calibration)

Bits 6~5 (RCM1~RCM0): IRC frequency selection

RCM1	RCM0	Frequency (MHz)
0	0	12
0	1	8 (default)
1	0	16
1	1	4

Bit 4 (DAS): Device Address Select for I^2C WTR

0: I^2C Slave address is at user's option (Word D) for WTR mode

1: I^2C Slave Address 0x77 for WTR mode (default)

Bits 3~2: Not used. Set to "**1**" all the time.

Bit 1 (OSC0): Main-oscillator mode select bit

Main-Oscillator Mode	OSC0
IRC (Internal RC oscillator mode; default) RCOUT (P54) functions as I/O pin	**1**
IRC (Internal RC oscillator mode) RCOUT (P54) functions as clock output pin	**0**

Bit 0 (RCOUT): System Clock Output enable bit in IRC mode

0: OSCO pin is open-drain

1: OSCO output instruction cycle time (default)

6.13.3 Code Option Register (Word 2)

Word 2															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	-	-	-	SC3	SC2	SC1	SC0	-	-	-	-	-	-	-	-
1	-	-	-	High	High	High	High	-	-	-	-	-	-	-	-
0	-	-	-	Low	Low	Low	Low	-	-	-	-	-	-	-	-
Default	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1

Bit 14: Not used. Set to "**0**" all the time.

Bits 13~12: Not used. Set to "**1**" all the time.

Bits 11~8 (SC3~SC0): Trim bits of sub-frequency IRC (auto calibration)

Bit 7: Not used. Set to "**1**" all the time.

Bit 6: Not used. Set to "**0**" all the time.

Bits 5~0: Not used. Set to "**1**" all the time.

6.13.4 Code Option Register (Word 3)

Word 3															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	-	-	-	-	-	-	-	-	-	ID5	ID4	ID3	ID2	ID1	ID0
1	-	-	-	-	-	-	-	-	-	Customer ID					
0	-	-	-	-	-	-	-	-	-						
Default	1	1	1	1	1	1	1	1	1						

Bits 14~6: Not used. Set to "**1**" all the time.

Bits 5~0 (ID5~ID0): Customer's ID Code

6.13.5 Code Option Register (Word D)

Word D															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	-	-	-	-	-	-	-	-	I2CS6	I2CS5	I2CS4	I2CS3	I2CS2	I2CS1	I2CS0
1	-	-	-	-	-	-	-	-	High	High	High	High	High	High	High
0	-	-	-	-		-	-	-	Low	Low	Low	Low	Low	Low	Low
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits 14~7: Not used. Set to "1" all the time.

Bits 6~0 (I2CS6~I2CS0): User setting Device Address for I^2C WTR

6.14 Instruction Set

Each instruction in the instruction set is a 15-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2, A", "ADD R2, A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2, A", "BS(C) R2, 6", "CLR R2", etc·). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

- "LCALL", "LJMP", "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Moreover, the instruction set has the following features:

1) Every bit of any register can be directly set, cleared, or tested.
2) The I/O register can be considered as general register. That is; the same instruction can operate on I/O register.

■ Instruction Set Table:

In the following Instruction Set table, the following symbols are used:

"**R**" *represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction.*

"**b**" *represents a bit field designator that selects the value for the bit which is located in the register "**R**", and affects operation.*

"**k**" *represents an 8 or 10-bit constant or literal value.*

Mnemonic	Operation	Affected Status
NOP	No Operation	None
DAA	Decimal Adjust A	C
SLEP	0 → WDT, Stop oscillator	T, P
WDTC	0 → WDT	T, P
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z, C, DC
SUB R,A	R-A → R	Z, C, DC
DECA R	R-1 → A	Z
DEC R	R-1 → R	Z
OR A,R	A ∨ R → A	Z
OR R,A	A ∨ R → R	Z
AND A,R	A & R → A	Z
AND R,A	A & R → R	Z
XOR A,R	A ⊕ R → A	Z
XOR R,A	A ⊕ R → R	Z
ADD A,R	A + R → A	Z, C, DC
ADD R,A	A + R → R	Z, C, DC
MOV A,R	R → A	Z
MOV R,R	R → R	Z
COMA R	/R → A	Z
COM R	/R → R	Z
INCA R	R+1 → A	Z
INC R	R+1 → R	Z
DJZA R	R-1 → A, skip if zero	None
DJZ R	R-1 → R, skip if zero	None
RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C

(Continuation)

Mnemonic	Operation	Affected Status
RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
SWAP R	R(0-3) ↔ R(4-7)	None
JZA R	R+1 → A, skip if zero	None
JZ R	R+1 → R, skip if zero	None
BC R,b	0 → R(b)	None <Note1>
BS R,b	1 → R(b)	None <Note2>
JBC R,b	if R(b)=0, skip	None
JBS R,b	if R(b)=1, skip	None
CALL k	PC+1 → [SP], (Page, k) → PC	None
JMP k	(Page, k) → PC	None
MOV A,k	k → A	None
OR A,k	A ∨ k → A	Z
AND A,k	A & k → A	Z
XOR A,k	A ⊕ k → A	Z
RETL k	k → A, [Top of Stack] → PC	None
SUB A,k	k-A → A	Z,C,DC
ADD A,k	K+A → A	Z,C,DC
SBANK k	K->R1(4)	None
GBANK k	K->R1(3:0)	None
LCALL k	Next instruction**:** k kkkk kkkk kkkk PC+1→[SP], k→PC	None
LJMP k	Next instruction**:** k kkkk kkkk kkkk K→PC	None
TBRD R	ROM[(TABPTR)] → R	None

Note:

1. *This instruction is not recommended for interrupt status register operation.*
   If user wants to clear Bit 0 for interrupt status register (ex. 0xF), the method recommended is shown below:
   MOV A,@0B11111110
   AND 0xF,A
2. *This instruction cannot operate under interrupt status register.*

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	VDD+0.3V
Output voltage	Vss-0.3V	to	VDD+0.3V
Working Voltage	2.5V	to	3.6V
Working Frequency	DC	to	16 MHz

8 DC Electrical Characteristics

■ **(Ta=25°C, VDD=3.6V±5%, VSS=0V)**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	IRC: VDD to 3.6 V	4 MHz, 12 MHz, 8kHz, 16 MHz	-	F	-	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
IRCE	Internal RC oscillator error per stage	-	-	±1	-	%
IRC1	IRC: VDD to 3.6V	RCM0:RCM1=1:1	-	4	-	MHz
IRC2	IRC: VDD to 3.6V	RCM0:RCM1=1:0	-	16	-	MHz
IRC3	IRC: VDD to 3.6V	RCM0:RCM1=0:1	-	8	-	MHz
IRC4	IRC: VDD to 3.6V	RCM0:RCM1=0:0	-	12	-	MHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	0.7Vdd	-	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	-0.3V	-	0.3Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.7Vdd	-	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V	-	0.3Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC, INT	0.7Vdd	-	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC, INT	-0.3V	-	0.3Vdd	V
IOH1	Output High Voltage (Ports 5, 6, 7, 8)	VOH = VDD-0.1VDD	-	-4.5	-	mA
IOH2	Output High Voltage (high drive) (Ports 5, 6, 7, 8)	VOH = VDD-0.1VDD	-	-8	-	mA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IOL1	Output Low Voltage (Ports 5, 6, 7, 8)	VOL = GND+0.1VDD	-	16	-	mA
IOL2	Output Low Voltage (high sink) (Ports 5, 6, 7, 8)	VOL = GND+0.1VDD	-	25	-	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	-	-75	-	µA
IPL	Pull-low current	Pull-low active, input pin at Vdd	-	40	-	µA
ISB1	Power down current (Sleep mode)	/RESET= 'High', Fm and Fs off. All input and I/O pins at VDD, Output pin floating, WDT disabled	-	4	-	µA
ISB2	Power down current (Sleep mode)	/RESET= 'High', Fm and Fs off. All input and I/O pins at VDD, Output pin floating, WDT enabled	-	5	-	µA
ISB3	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs=64K/16kHz (IRC type), Output pin floating, WDT disabled,	-	5	-	µA
ISB4	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs=64K/16kHz (IRC type), Output pin floating, WDT enabled	-	5	-	µA
ICC1	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=64K/16kHz (IRC type), Output pin floating, WDT disabled	-	40	-	µA
ICC2	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=64K/16kHz (IRC type), Output pin floating, WDT enabled	-	41	-	µA
ICC3	Operating supply current (Normal mode)	/RESET= 'High', Fm=4MHz (IRC type), Fs is on, Output pin floating, WDT enabled	-	1	-	mA
ICC4	Operating supply current (Normal mode)	/RESET= 'High', Fm=16MHz (IRC type), Fs is on, Output pin floating, WDT enabled	-	2.8	-	mA

NOTE

- *The above parameters are theoretical values only and have not been tested or verified.*
- *Data under the "Min.", "Typ.", and "Max." columns are based on theoretical results at 25℃. These data are for design reference only and have not been tested or verified.*

9 AC Electrical Characteristics

■ **(eKTF5705 -40□Ta□85°C, VDD=3.6V, VSS=0V)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	-	45	50	55	%
Tins	Instruction cycle time	RC type	500	-	DC	ns
Ttcc	TCC input period	-	(Tins+20)/N*	-	-	ns
Tdrh	Device reset hold time	-	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25°C	2000	-	-	ns
Twdt	Watchdog timer period	Ta = 25°C	11.3	16.2	21.6	ms
Tset	Input pin setup time	-	-	0		ns
Thold	Input pin hold time	-	15	20	25	ns
Tdelay	Output pin delay time	Cload=20pF	45	50	55	ns

* ***N:*** *Selected prescaler ratio*

NOTE

- *The above parameters are theoretical values only and have not been tested or verified.*
- *Data under the "Min.", "Typ.", and "Max." columns are based on theoretical results at 25℃. These data are for design reference only and have not been tested or verified.*

APPENDIX

A Package Type

MCU	Package Type	Pin Count	Package Size
eKTF5705QN24J/S	QFN	24 pins	4x4x0.8 mm
eKTF5705SO24J/S	SOP	24 pins	300 mil

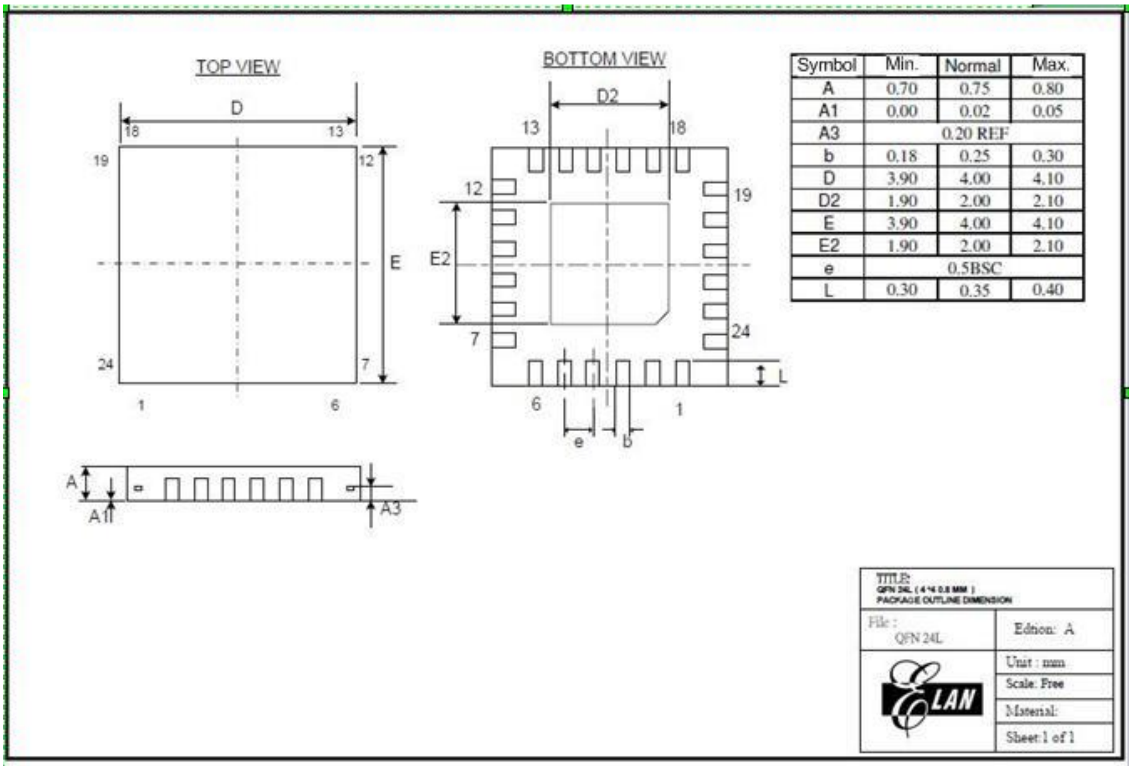
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

The Pb contents are less 100ppm and comply with Sony specifications.

Part No.	eKTF5705 S/J
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point(°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

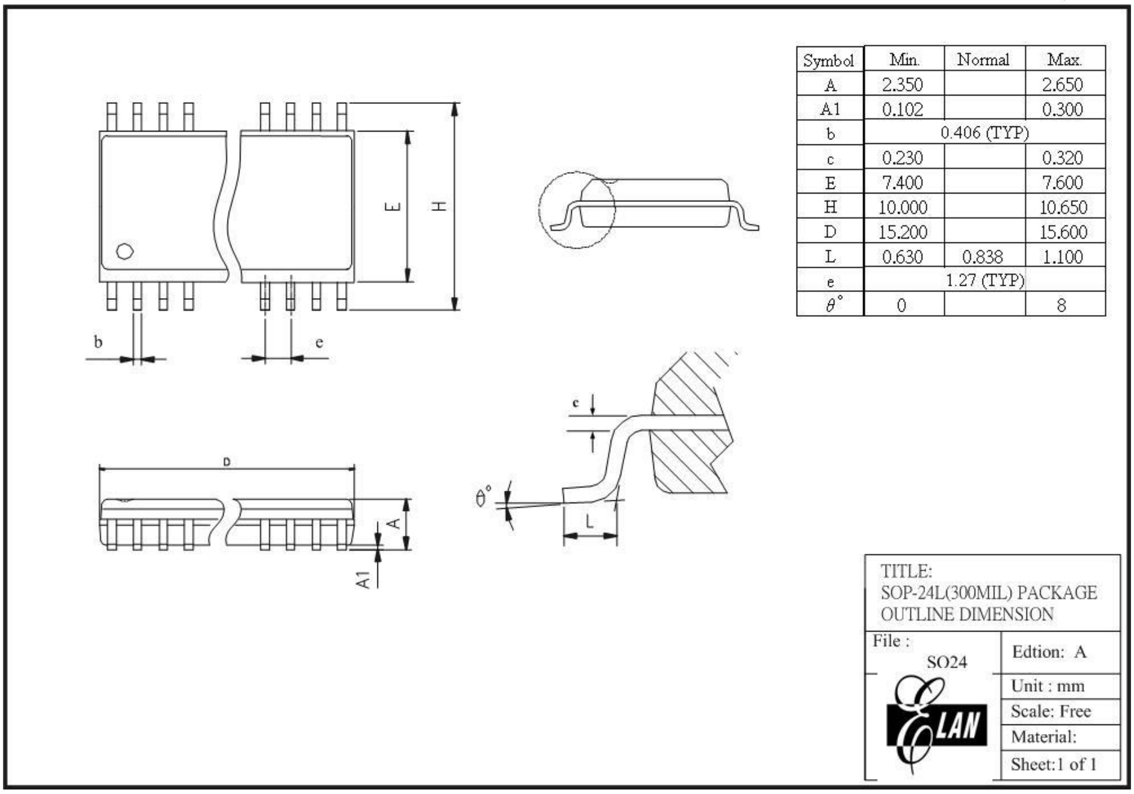
B Package Information

B.1 eKTF5705QN24



Symbol	Min.	Normal	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	1.90	2.00	2.10
E	3.90	4.00	4.10
E2	1.90	2.00	2.10
e		0.5BSC	
L	0.30	0.35	0.40

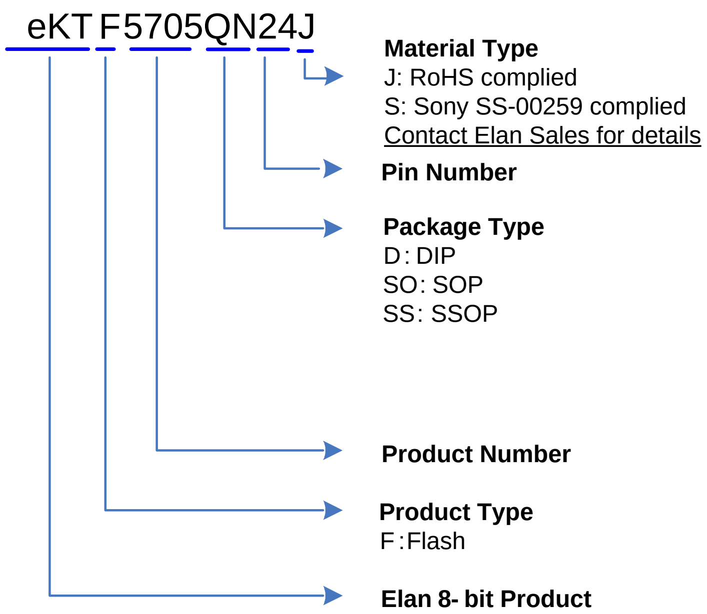
Figure B-1 eKTF5705 24-pin QFN Package Type



Symbol	Min.	Normal	Max.
A	2.350		2.650
A1	0.102		0.300
b		0.406 (TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	15.200		15.600
L	0.630	0.838	1.100
e		1.27 (TYP)	
θ°	0		8

Figure B-2 eKTF5705 24-pin SOP Package Type

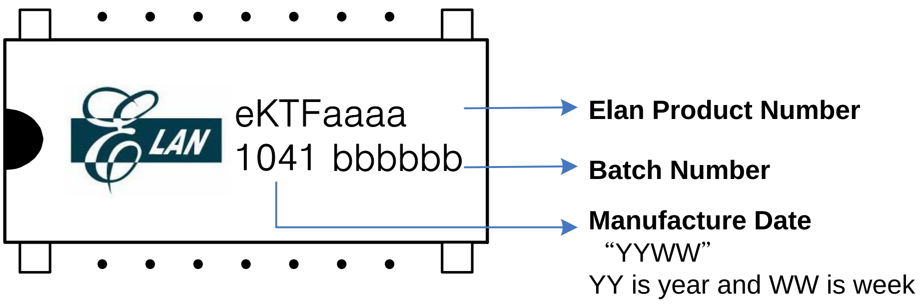
C Ordering and Manufacturing Information



For example

eKTF5705QN24J

is eKTF5705 with Flash program memory , in 24-pin QFN package



Ordering Code