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FAIRCHILD SEMICONDUCTOR®

September 2012

FSL206MR
Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche-Rugged SenseFET: 650V
- Precision Fixed Operating Frequency: 67kHz
- No-Load <150mW at 265V_{AC} without Bias Winding; <25mW with Bias Winding for FSL206MR, <30mW with Bias Winding for FSL206MRBN
- No Need for Auxiliary Bias Winding
- Frequency Modulation for Attenuating EMI
- Line Under-Voltage Protection (LUVP)
- Pulse-by-Pulse Current Limiting
- Low Under-Voltage Lockout (UVLO)
- Ultra-Low Operating Current: 300μA
- Built-In Soft-Start and Startup Circuit
- Various Protections: Overload Protection (OLP), Over-Voltage Protection (OVP), Thermal Shutdown (TSD), Abnormal Over-Current Protection (AOCP) Auto-Restart Mode for All Protections

Applications

- SMPS for STB, DVD, and DVCD Player
- SMPS for Auxiliary Power

Related Resources

- *Fairchild Power Supply WebDesigner – Flyback Design and Simulation – In Minutes at No Expense*
- *AN-4137 — Design Guidelines for Offline Flyback Converters Using FPS™*
- *AN-4141 — Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications*
- *AN-4147 — Design Guidelines for RCD Snubber of Flyback*
- *AN-4150 — Design Guidelines for Flyback Converters Using FSQ-Series Fairchild Power Switch (FPS™)*

Description

The FSL206MR integrated Pulse-Width Modulator (PWM) and SenseFET is specifically designed for high-performance offline Switched-Mode Power Supplies (SMPS) while minimizing external components. This device integrates high-voltage power regulators that combine an avalanche-rugged SenseFET with a Current-Mode PWM control block.

The integrated PWM controller includes: a 7.8V regulator, eliminating the need for auxilliary bias winding; Under-Voltage Lockout (UVLO) protection; Leading-Edge Blanking (LEB); an optimized gate turn-on/turn-off driver; EMI attenuator; Thermal Shutdown (TSD) protection; temperature-compensated precision current sources for loop compensation; soft-start during startup; and fault-protection circuitry such as Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), and Line Under-Voltage Protection (LUVP).

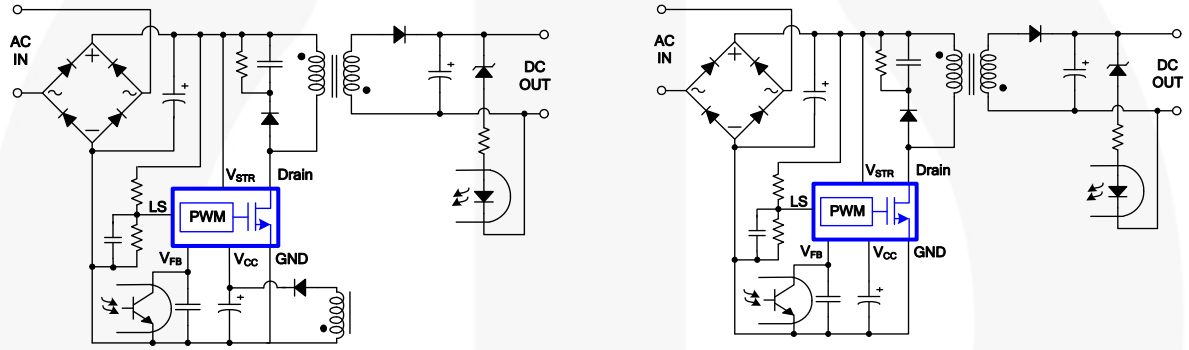
The internal high-voltage startup switch and the Burst-Mode operation with very low operating current reduce the power loss in Standby Mode. As a result, it is possible to reach a power loss of 150mW with no bias winding and 25mW (for FSL206MR) or 30mW (for FSL206MRBN) with a bias winding under no-load conditions when the input voltage is 265V_{AC}.

Ordering Information

Part Number	Operating Temperature	Top Mark	PKG	Packing Method	Output Power Table[1]			
					Current Limit	$R_{DS(ON),MAX}$	$230V_{AC}$ ±15%[2]	85 ~ $265V_{AC}$
							Open Frame[3]	Open Frame[3]
FSL206MRN	-40 ~ 115°C	FSL206MR	8-DIP	Rail	0.6A	19Ω	12W	7W
FSL206MRL			8-LSOP					
FSL206MRBN		L206MRB	8-DIP					

Notes:
1. The junction temperature can limit the maximum output power.
2. $230V_{AC}$ or $100/115V_{AC}$ with doubler. The maximum power with CCM operation.
3. Maximum practical continuous power in an open-frame design at 50°C ambient.

Application Diagram



(a) With Bias Winding (b) Without Bias Winding

Figure 1. Typical Application

Internal Block Diagram

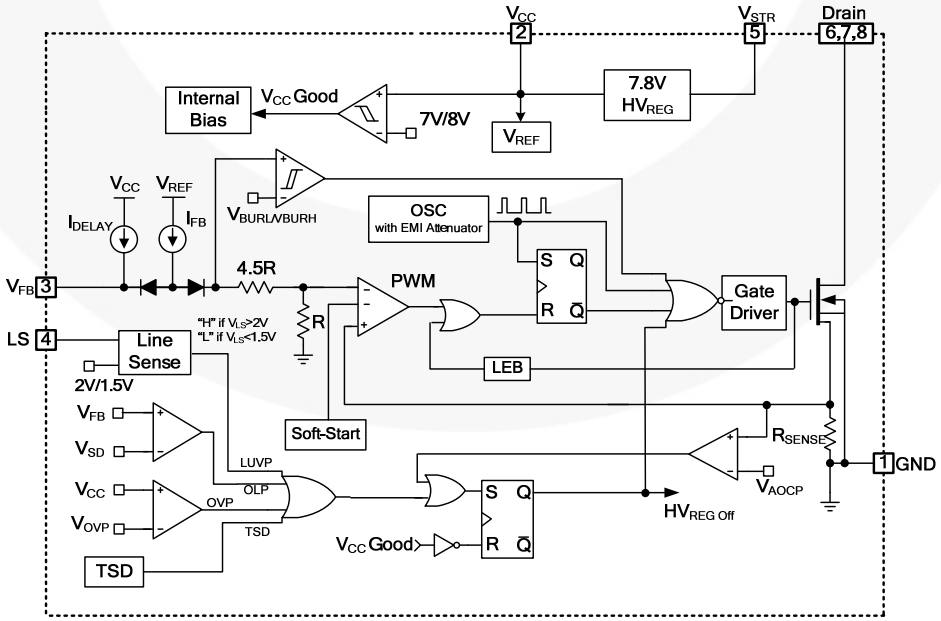


Figure 2. Internal Block Diagram

Pin Configuration

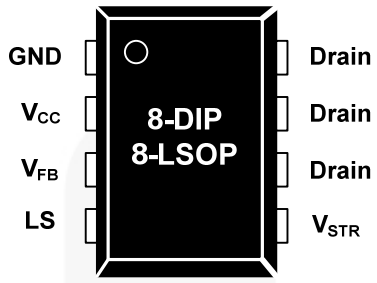


Figure 3. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GND	**Ground**. SenseFET source terminal on primary side and internal control ground.
2	V_{CC}	**Positive Supply Voltage Input**. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (V_{STR}) via an internal switch during startup *(see Internal Block Diagram section)*. It is not until V_{CC} reaches the UVLO upper threshold (8V) that the internal startup switch opens and device power is supplied via the auxiliary transformer winding.
3	V_{FB}	**Feedback Voltage**. Non-inverting input to the PWM comparator, with a 0.11mA current source connected internally and a capacitor and opto-coupler typically connected externally. There is a delay while charging external capacitor C_{FB} from 2.4V to 5V using an internal 2.7μA current source. This delay prevents false triggering under transient conditions, but allows the protection mechanism to operate under true overload conditions.
4	LS	Line Sense Pin. This pin is used to protect the device when the input voltage is lower than the rated input voltage range. If this pin is not used, connect to ground.
5	V_{STR}	**Startup**. Connected to the rectified AC line voltage source. At startup, the internal switch supplies internal bias and charges an external storage capacitor placed between the V_{CC} pin and ground. Once V_{CC} reaches 8V, all internal blocks are activated. After that, the internal high-voltage regulator (HV REG) turns on and off irregularly to maintain V_{CC} at 7.8V.
6, 7, 8	Drain	**Drain**. Designed to connect directly to the primary lead of the transformer and capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer decreases leakage inductance.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25°C unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
V_{STR}	V_{STR} Pin Voltage	-0.3	650.0	V
V_{DS}	Drain Pin Voltage	-0.3	650.0	V
V_{CC}	Supply Voltage		26	V
V_{LS}	LS Pin Voltage	-0.3	Internally Clamped Voltage(4)	V
V_{FB}	Feedback Voltage Range	-0.3	Internally Clamped Voltage(4)	V
I_{DM}	Drain Current Pulsed(5)		1.5	A
E_{AS}	Single-Pulsed Avalanche Energy(6)		11	mJ
P_D	Total Power Dissipation		1.3	W
T_J	Operating Junction Temperature	-40	+150	°C
T_A	Operating Ambient Temperature	-40	+125	°C
T_{STG}	Storage Temperature	-55	+150	°C
ESD	Human Body Model, JESD22-A114		4	KV
	Charged Device Model, JESD22-C101		2	

Notes:

4. V_{FB} is clamped by internal clamping diode (13V I_{CLAMP_MAX} < 100μA). After shutdown, before V_{CC} reaching V_{STOP}, $V_{SD} < V_{FB} < V_{CC}$.
5. Repetitive rating: pulse-width limited by maximum junction temperature.
6. L=21mH, starting T_J=25°C.

Thermal Impedance

T_A=25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance(7)	93	°C/W

Notes:

7. JEDEC recommended environment, JESD51-2 and test board, JESD51-10 with minimum land pattern for 8DIP and JESD51-3 with minimum land pattern for 8LSOP.

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
SenseFET Section							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{CC} = 0V, I_D = 250μA		650			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650V, V_{GS} = 0V				50	μA
		V_{DS} = 520V, V_{GS} = 0V, T_A = 125°C[8]				250	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[9]	V_{GS} = 10V, I_D = 0.3A			14	19	Ω
C_{iSS}	Input Capacitances	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz			162		pF
C_{OSS}	Output Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz			14.9		pF
C_{RSS}	Reverse Transfer Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz			2.7		pF
t_r	Rise Time	V_{DS} = 325V, I_D = 0.5A, R_G = 25Ω			6.1		ns
t_f	Fall Time	V_{DS} = 325V, I_D = 0.5A, R_G = 25Ω			43.6		ns
Control Section							
f_{OSC}	Switching Frequency	V_{FB} = 4V, V_{CC} = 10V		61	67	73	KHz
Δf_{OSC}	Switching Frequency Variation	-25°C < T_J < 85°C			±5	±10	%
f_M	Frequency Modulation[8]				±3		KHz
D_{MAX}	Maximum Duty Cycle	V_{FB} = 4V, V_{CC} = 10V		66	72	78	%
D_{MIN}	Minimum Duty Cycle	V_{FB} = 0V, V_{CC} = 10V		0	0	0	%
V_{START}	UVLO Threshold Voltage	V_{FB} = 0V, V_{CC} Sweep		7	8	9	V
V_{STOP}		After Turn On		6	7	8	V
I_{FB}	Feedback Source Current	V_{FB}= 0V, V_{CC} = 10V		90	110	130	μA
$t_{S/S}$	Internal Soft-Start Time	V_{FB} = 4V, V_{CC} = 10V		10	15	20	ms
Burst Mode Section							
V_{BURH}	Burst-Mode HIGH Threshold Voltage	V_{CC} = 10V, V_{FB} Increase	FSL206MR	0.66	0.83	1.00	V
			FSL206MRB	0.40	0.50	0.60	V
V_{BURL}	Burst-Mode LOW Threshold Voltage	V_{CC} = 10V, V_{FB} Decrease	FSL206MR	0.59	0.74	0.89	V
			FSL206MRB	0.28	0.35	0.42	V
HYS_{BUR}	Burst-Mode Hysteresis		FSL206MR		90		mV
			FSL206MRB		150		mV
Protection Section							
I_{LIM}	Peak Current Limit	V_{FB} = 4V, di/dt = 300mA/μs, V_{CC} = 10V		0.54	0.60	0.66	A
t_{CLD}	Current Limit Delay[8]				100		ns
V_{SD}	Shutdown Feedback Voltage	V_{CC} = 10V		4.5	5.0	5.5	V
I_{DELAY}	Shutdown Delay Current	V_{FB} = 4V		2.1	2.7	3.3	μA
t_{LEB}	Leading-Edge Blanking Time[8]			250			ns
V_{AOCP}	Abnormal Over-Current Protection[8]				0.7		V
V_{OVP}	Over-Voltage Protection	V_{FB} = 4V, V_{CC} Increase		23.0	24.5	26.0	V
V_{LS_OFF}	Line-Sense Protection On to Off	V_{FB} = 3V, V_{CC} = 10V, V_{LS} Decrease		1.9	2.0	2.1	V
V_{LS_ON}	Line-Sense Protection Off to On	V_{FB} = 3V, V_{CC} = 10V, V_{LS} Increase		1.4	1.5	1.6	V
TSD	Thermal Shutdown Temperature[8]			125	135	150	°C
HYS_{TSD}	TSD Hysteresis Temperature[8]				60		°C

Continued on the following page…

Electrical Characteristics (Continued)

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
High Voltage Regulator Section						
V_{HVR}	HV Regulator Voltage	V_{FB} = 0V, V_{STR} = 40V		7.8		V
Total Device Section						
I_{OP1}	Operating Supply Current (Control Part Only, without Switching)	V_{CC} = 15V, 0V<V_{FB}<V_{BURL}		0.3	0.5	mA
I_{OP2}	Operating Supply Current (Control Part Only, without Switching)	V_{CC} = 8V, 0V<V_{FB}<V_{BURL}		0.25	0.45	mA
I_{OP3}	Operating Supply Current[8] (While Switching)	V_{CC} = 15V, V_{BURL}<V_{FB}<V_{SD}			1.3	mA
I_{CH}	Startup Charging Current	V_{CC} = 0V, V_{STR} > 40V	1.6	1.9	2.2	mA
I_{START}	Startup Current	V_{CC} = Before V_{START}, V_{FB} = 0V		100	150	μA
V_{STR}	Minimum V_{STR} Supply Voltage	V_{CC} = V_{FB} = 0V, V_{STR} Increase		26		V

Notes:

8. Though guaranteed by design, not 100% tested in production.
9. Pulse test: pulse width=300ms, duty cycle=2%.

Typical Performance Characteristics

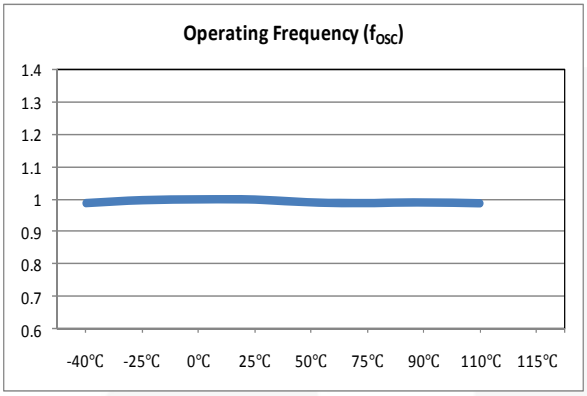


Figure 4. Operating Frequency vs. Temperature

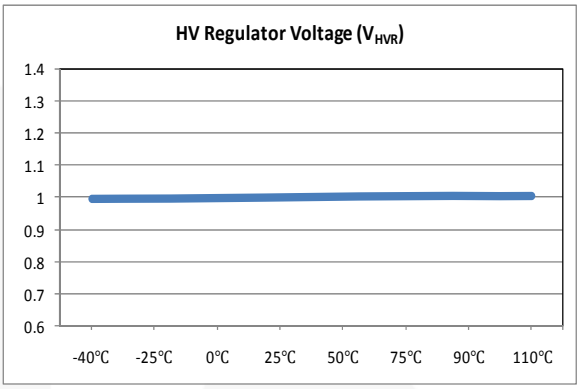


Figure 5. HV Regulator Voltage vs. Temperature

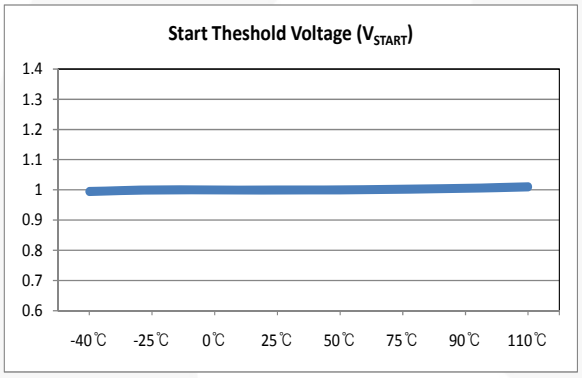


Figure 6. Start Threshold Voltage vs. Temperature

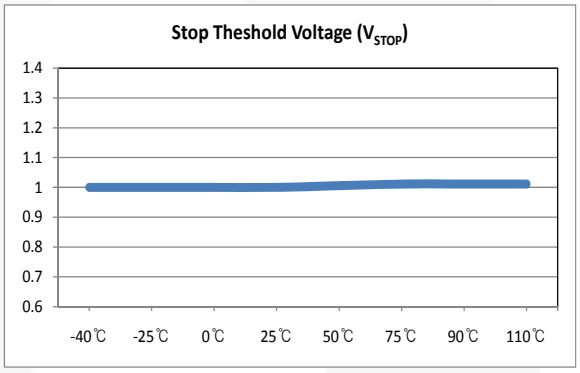


Figure 7. Stop Threshold Voltage vs. Temperature

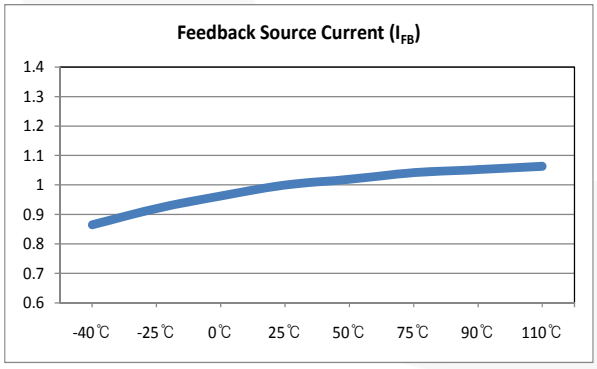


Figure 8. Feedback Source Current vs. Temperature

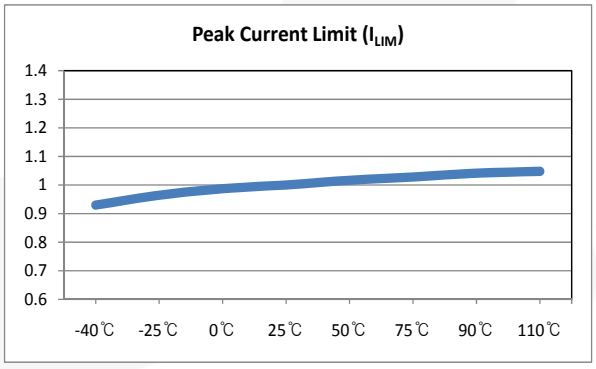


Figure 9. Peak Current Limit vs. Temperature