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## FSL206MR

### Green Mode Fairchild Power Switch (FPS™)

#### Features

- Internal Avalanche-Rugged SenseFET: 650V
- Precision Fixed Operating Frequency: 67kHz
- No-Load <150mW at 265V<sub>AC</sub> without Bias Winding; <25mW with Bias Winding for FSL206MR, <30mW with Bias Winding for FSL206MRBN
- No Need for Auxiliary Bias Winding
- Frequency Modulation for Attenuating EMI
- Line Under-Voltage Protection (LUVF)
- Pulse-by-Pulse Current Limiting
- Low Under-Voltage Lockout (UVLO)
- Ultra-Low Operating Current: 300μA
- Built-In Soft-Start and Startup Circuit
- Various Protections: Overload Protection (OLP), Over-Voltage Protection (OVP), Thermal Shutdown (TSD), Abnormal Over-Current Protection (AOCP) Auto-Restart Mode for All Protections

#### Applications

- SMPS for STB, DVD, and DVCD Player
- SMPS for Auxiliary Power

#### Related Resources

- [Fairchild Power Supply WebDesigner – Flyback Design and Simulation – In Minutes at No Expense](#)
- [AN-4137 — Design Guidelines for Offline Flyback Converters Using FPS™](#)
- [AN-4141 — Troubleshooting and Design Tips for Fairchild Power Switch \(FPS™\) Flyback Applications](#)
- [AN-4147 — Design Guidelines for RCD Snubber of Flyback](#)
- [AN-4150 — Design Guidelines for Flyback Converters Using FSQ-Series Fairchild Power Switch \(FPS™\)](#)

#### Description

The FSL206MR integrated Pulse-Width Modulator (PWM) and SenseFET is specifically designed for high-performance offline Switched-Mode Power Supplies (SMPS) while minimizing external components. This device integrates high-voltage power regulators that combine an avalanche-rugged SenseFET with a Current-Mode PWM control block.

The integrated PWM controller includes: a 7.8V regulator, eliminating the need for auxiliary bias winding; Under-Voltage Lockout (UVLO) protection; Leading-Edge Blanking (LEB); an optimized gate turn-on/turn-off driver; EMI attenuator; Thermal Shutdown (TSD) protection; temperature-compensated precision current sources for loop compensation; soft-start during startup; and fault-protection circuitry such as Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), and Line Under-Voltage Protection (LUVF).

The internal high-voltage startup switch and the Burst-Mode operation with very low operating current reduce the power loss in Standby Mode. As a result, it is possible to reach a power loss of 150mW with no bias winding and 25mW (for FSL206MR) or 30mW (for FSL206MRBN) with a bias winding under no-load conditions when the input voltage is 265V<sub>AC</sub>.

## Ordering Information

Part Number	Operating Temperature	Top Mark	PKG	Packing Method	Output Power Table <sup>(1)</sup>			
					Current Limit	$R_{DS(ON),MAX}$	230V <sub>AC</sub> ±15% <sup>(2)</sup>	85 ~ 265V <sub>AC</sub>
							Open Frame <sup>(3)</sup>	Open Frame <sup>(3)</sup>
FSL206MRN	-40 ~ 115°C	FSL206MR	8-DIP	Rail	0.6A	19Ω	12W	7W
FSL206MRL			8-LSOP					
FSL206MRBN		L206MRB	8-DIP					

### Notes:

1. The junction temperature can limit the maximum output power.
2. 230V<sub>AC</sub> or 100/115V<sub>AC</sub> with doubler. The maximum power with CCM operation.
3. Maximum practical continuous power in an open-frame design at 50°C ambient.

## Application Diagram

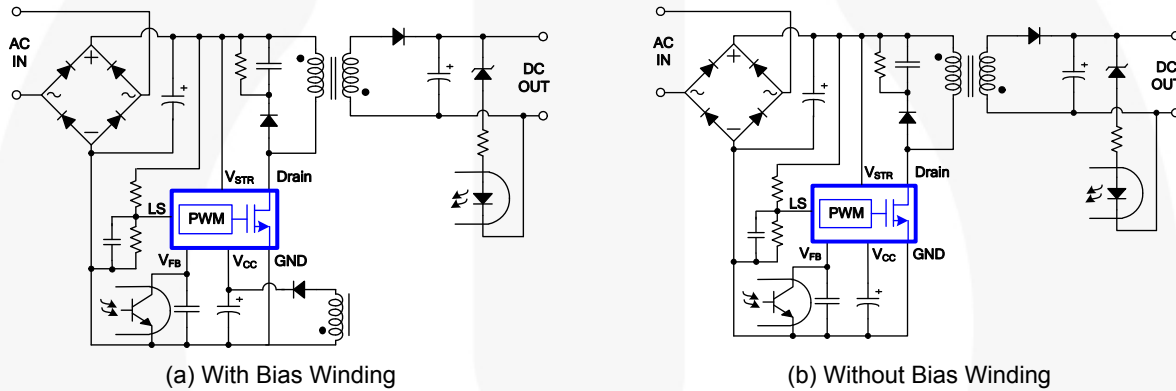


Figure 1. Typical Application

## Internal Block Diagram

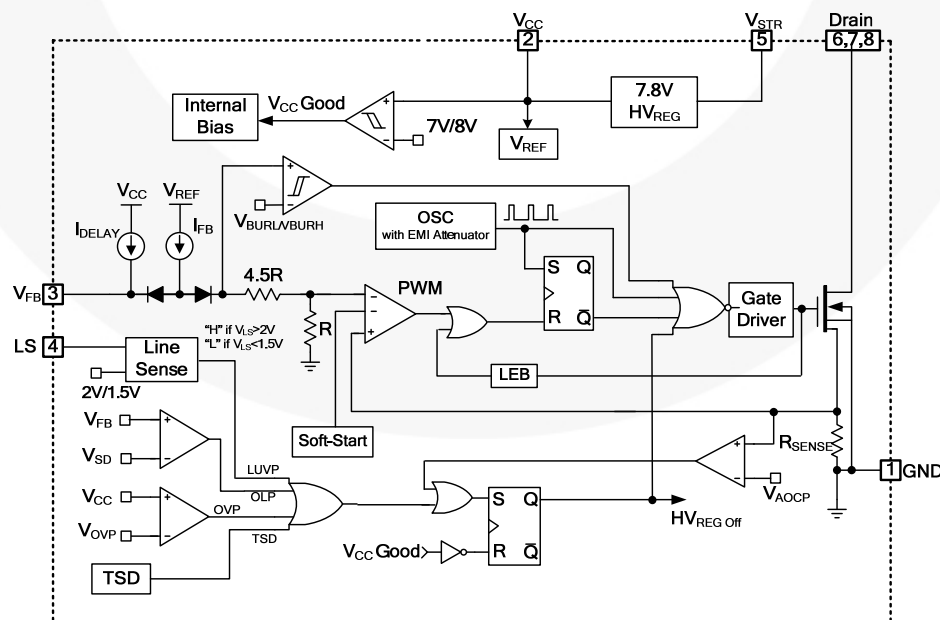


Figure 2. Internal Block Diagram

## Pin Configuration

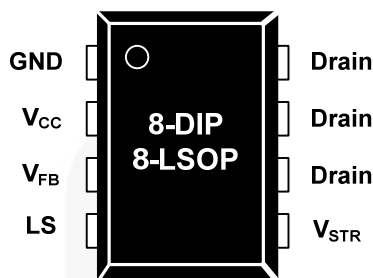


Figure 3. Pin Configuration

## Pin Definitions

Pin #	Name	Description
1	GND	<b>Ground.</b> SenseFET source terminal on primary side and internal control ground.
2	$V_{CC}$	<b>Positive Supply Voltage Input.</b> Although connected to an auxiliary transformer winding, current is supplied from pin 5 ( $V_{STR}$ ) via an internal switch during startup (see <i>Internal Block Diagram</i> section). It is not until $V_{CC}$ reaches the UVLO upper threshold (8V) that the internal startup switch opens and device power is supplied via the auxiliary transformer winding.
3	$V_{FB}$	<b>Feedback Voltage.</b> Non-inverting input to the PWM comparator, with a 0.11mA current source connected internally and a capacitor and opto-coupler typically connected externally. There is a delay while charging external capacitor $C_{FB}$ from 2.4V to 5V using an internal 2.7μA current source. This delay prevents false triggering under transient conditions, but allows the protection mechanism to operate under true overload conditions.
4	LS	<b>Line Sense Pin.</b> This pin is used to protect the device when the input voltage is lower than the rated input voltage range. If this pin is not used, connect to ground.
5	$V_{STR}$	<b>Startup.</b> Connected to the rectified AC line voltage source. At startup, the internal switch supplies internal bias and charges an external storage capacitor placed between the $V_{CC}$ pin and ground. Once $V_{CC}$ reaches 8V, all internal blocks are activated. After that, the internal high-voltage regulator (HV REG) turns on and off irregularly to maintain $V_{CC}$ at 7.8V.
6, 7, 8	Drain	<b>Drain.</b> Designed to connect directly to the primary lead of the transformer and capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer decreases leakage inductance.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
$V_{STR}$	$V_{STR}$ Pin Voltage	-0.3	650.0	V
$V_{DS}$	Drain Pin Voltage	-0.3	650.0	V
$V_{CC}$	Supply Voltage		26	V
$V_{LS}$	LS Pin Voltage	-0.3	Internally Clamped Voltage <sup>(4)</sup>	V
$V_{FB}$	Feedback Voltage Range	-0.3	Internally Clamped Voltage <sup>(4)</sup>	V
$I_{DM}$	Drain Current Pulsed <sup>(5)</sup>		1.5	A
$E_{AS}$	Single-Pulsed Avalanche Energy <sup>(6)</sup>		11	mJ
$P_D$	Total Power Dissipation		1.3	W
$T_J$	Operating Junction Temperature	-40	+150	$^\circ\text{C}$
$T_A$	Operating Ambient Temperature	-40	+125	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-55	+150	$^\circ\text{C}$
ESD	Human Body Model, JESD22-A114		4	KV
	Charged Device Model, JESD22-C101		2	

### Notes:

- $V_{FB}$  is clamped by internal clamping diode ( $13\text{V } I_{CLAMP\_MAX} < 100\mu\text{A}$ ). After shutdown, before  $V_{CC}$  reaching  $V_{STOP}$ ,  $V_{SD} < V_{FB} < V_{CC}$ .
- Repetitive rating; pulse-width limited by maximum junction temperature.
- $L=21\text{mH}$ , starting  $T_J=25^\circ\text{C}$ .

## Thermal Impedance

$T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Value	Unit
$\theta_{JA}$	Junction-to-Ambient Thermal Impedance <sup>(7)</sup>	93	$^\circ\text{C/W}$

### Notes:

- JEDEC recommended environment, JESD51-2 and test board, JESD51-10 with minimum land pattern for 8DIP and JESD51-3 with minimum land pattern for 8LSOP.

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	
SenseFET Section							
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>CC</sub> = 0V, I <sub>D</sub> = 250μA	650			V	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 650V, V <sub>GS</sub> = 0V			50	μA	
		V <sub>DS</sub> = 520V, V <sub>GS</sub> = 0V, T <sub>A</sub> = 125°C <sup>(8)</sup>			250	μA	
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance <sup>(9)</sup>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 0.3A		14	19	Ω	
C <sub>ISS</sub>	Input Capacitances	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1MHz		162		pF	
C <sub>OSS</sub>	Output Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1MHz		14.9		pF	
C <sub>RSS</sub>	Reverse Transfer Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1MHz		2.7		pF	
t <sub>r</sub>	Rise Time	V <sub>DS</sub> = 325V, I <sub>D</sub> = 0.5A, R <sub>G</sub> = 25Ω		6.1		ns	
t <sub>f</sub>	Fall Time	V <sub>DS</sub> = 325V, I <sub>D</sub> = 0.5A, R <sub>G</sub> = 25Ω		43.6		ns	
Control Section							
f <sub>OSC</sub>	Switching Frequency	V <sub>FB</sub> = 4V, V <sub>CC</sub> = 10V	61	67	73	KHz	
Δf <sub>OSC</sub>	Switching Frequency Variation	-25°C < T <sub>J</sub> < 85°C		±5	±10	%	
f <sub>M</sub>	Frequency Modulation <sup>(8)</sup>			±3		KHz	
D <sub>MAX</sub>	Maximum Duty Cycle	V <sub>FB</sub> = 4V, V <sub>CC</sub> = 10V	66	72	78	%	
D <sub>MIN</sub>	Minimum Duty Cycle	V <sub>FB</sub> = 0V, V <sub>CC</sub> = 10V	0	0	0	%	
V <sub>START</sub>	UVLO Threshold Voltage	V <sub>FB</sub> = 0V, V <sub>CC</sub> Sweep	7	8	9	V	
V <sub>STOP</sub>		After Turn On	6	7	8	V	
I <sub>FB</sub>	Feedback Source Current	V <sub>FB</sub> = 0V, V <sub>CC</sub> = 10V	90	110	130	μA	
t <sub>S/S</sub>	Internal Soft-Start Time	V <sub>FB</sub> = 4V, V <sub>CC</sub> = 10V	10	15	20	ms	
Burst Mode Section							
V <sub>BURH</sub>	Burst-Mode HIGH Threshold Voltage	V <sub>CC</sub> = 10V, V <sub>FB</sub> Increase	FSL206MR	0.66	0.83	1.00	V
			FSL206MRB	0.40	0.50	0.60	V
V <sub>BURL</sub>	Burst-Mode LOW Threshold Voltage	V <sub>CC</sub> = 10V, V <sub>FB</sub> Decrease	FSL206MR	0.59	0.74	0.89	V
			FSL206MRB	0.28	0.35	0.42	V
HYS <sub>BUR</sub>	Burst-Mode Hysteresis		FSL206MR		90		mV
			FSL206MRB		150		mV
Protection Section							
I <sub>LIM</sub>	Peak Current Limit	V <sub>FB</sub> = 4V, di/dt = 300mA/μs, V <sub>CC</sub> = 10V	0.54	0.60	0.66	A	
t <sub>CLD</sub>	Current Limit Delay <sup>(8)</sup>			100		ns	
V <sub>SD</sub>	Shutdown Feedback Voltage	V <sub>CC</sub> = 10V	4.5	5.0	5.5	V	
I <sub>DELAY</sub>	Shutdown Delay Current	V <sub>FB</sub> = 4V	2.1	2.7	3.3	μA	
t <sub>LEB</sub>	Leading-Edge Blanking Time <sup>(8)</sup>		250			ns	
V <sub>AOCP</sub>	Abnormal Over-Current Protection <sup>(8)</sup>			0.7		V	
V <sub>OVP</sub>	Over-Voltage Protection	V <sub>FB</sub> = 4V, V <sub>CC</sub> Increase	23.0	24.5	26.0	V	
V <sub>LS_OFF</sub>	Line-Sense Protection On to Off	V <sub>FB</sub> = 3V, V <sub>CC</sub> = 10V, V <sub>LS</sub> Decrease	1.9	2.0	2.1	V	
V <sub>LS_ON</sub>	Line-Sense Protection Off to On	V <sub>FB</sub> = 3V, V <sub>CC</sub> = 10V, V <sub>LS</sub> Increase	1.4	1.5	1.6	V	
TSD	Thermal Shutdown Temperature <sup>(8)</sup>		125	135	150	°C	
HYS <sub>TSD</sub>	TSD Hysteresis Temperature <sup>(8)</sup>			60		°C	

Continued on the following page...

**Electrical Characteristics** (Continued) $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>High Voltage Regulator Section</b>						
$V_{HVR}$	HV Regulator Voltage	$V_{FB} = 0V, V_{STR} = 40V$		7.8		V
<b>Total Device Section</b>						
$I_{OP1}$	Operating Supply Current (Control Part Only, without Switching)	$V_{CC} = 15V, 0V < V_{FB} < V_{BURL}$		0.3	0.5	mA
$I_{OP2}$	Operating Supply Current (Control Part Only, without Switching)	$V_{CC} = 8V, 0V < V_{FB} < V_{BURL}$		0.25	0.45	mA
$I_{OP3}$	Operating Supply Current <sup>(8)</sup> (While Switching)	$V_{CC} = 15V, V_{BURL} < V_{FB} < V_{SD}$			1.3	mA
$I_{CH}$	Startup Charging Current	$V_{CC} = 0V, V_{STR} > 40V$	1.6	1.9	2.2	mA
$I_{START}$	Startup Current	$V_{CC} = \text{Before } V_{START}, V_{FB} = 0V$		100	150	$\mu\text{A}$
$V_{STR}$	Minimum $V_{STR}$ Supply Voltage	$V_{CC} = V_{FB} = 0V, V_{STR}$ Increase		26		V

**Notes:**

8. Though guaranteed by design, not 100% tested in production.
9. Pulse test: pulse width=300ms, duty cycle=2%.

## Typical Performance Characteristics

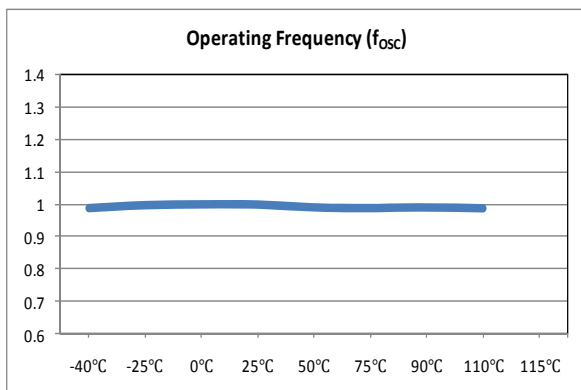


Figure 4. Operating Frequency vs. Temperature

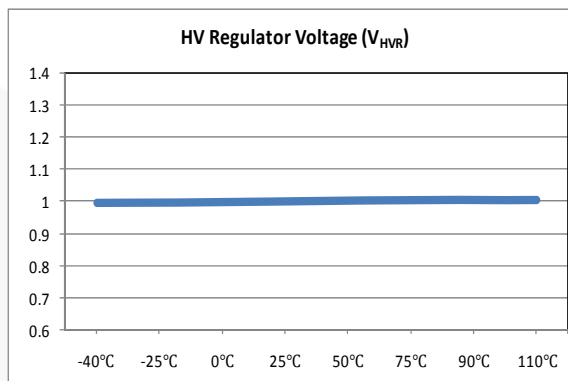


Figure 5. HV Regulator Voltage vs. Temperature

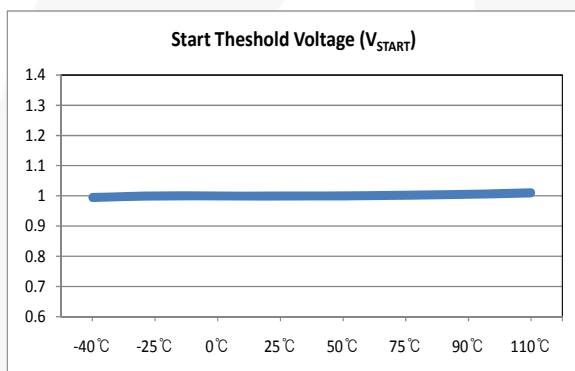


Figure 6. Start Threshold Voltage vs. Temperature

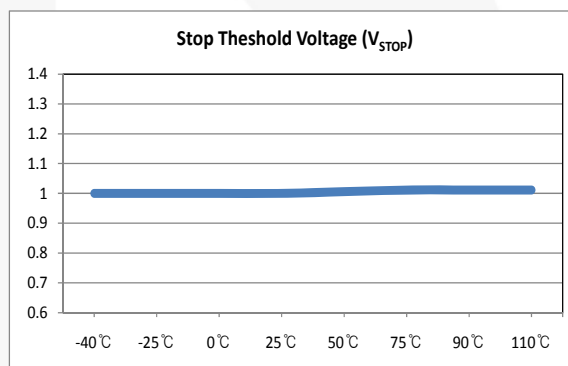


Figure 7. Stop Threshold Voltage vs. Temperature

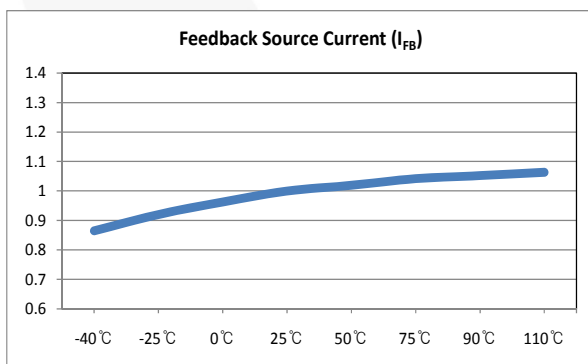


Figure 8. Feedback Source Current vs. Temperature

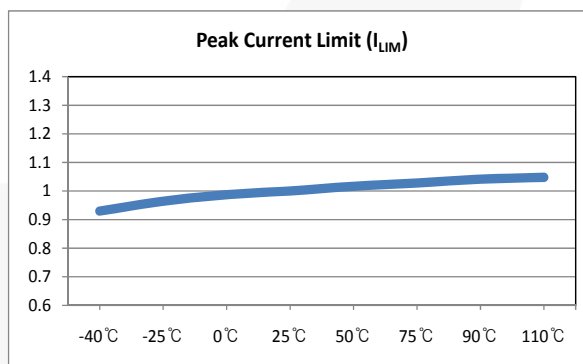


Figure 9. Peak Current Limit vs. Temperature