# INAx126 MicroPower Instrumentation Amplifier Single and Dual Versions

## 1 Features

- Low Quiescent Current: 175 μA/channel
- Wide Supply Range: ±1.35 V to ±18 V
- Low Offset Voltage: 250-μV Maximum
- Low Offset Drift: 3-μV/°C Maximum
- Low Noise: 35 nV/√Hz
- Low Input Bias Current: 25-nA Maximum
- 8-Pin PDIP, SOIC, VSSOP Surface-Mount Dual: 16-Pin PDIP, SOIC, SSOP

## 2 Applications

- Industrial Sensor Amplifiers: Bridges, RTDs, Thermocouples
- Physiological Amplifiers: ECGs, EEGs, EMGs
- Multi-Channel Data Acquisition
- Portable, Battery-Operated Systems

## 3 Description

The INA126 and INA2126 are precision instrumentation amplifiers for accurate, low noise differential-signal acquisition. Their two-op-amp design provides excellent performance with low quiescent current (175 μA/channel). Combined with a wide operating voltage range of ±1.35 V to ±18 V, makes the INAx126 ideal for portable instrumentation and data acquisition systems.

Gain can be set from 5 V/V to 10000 V/V with a single external resistor. Laser-trimmed input circuitry provides low offset voltage (250-μV maximum), low offset voltage drift (3-μV/°C maximum), and excellent common-mode rejection.

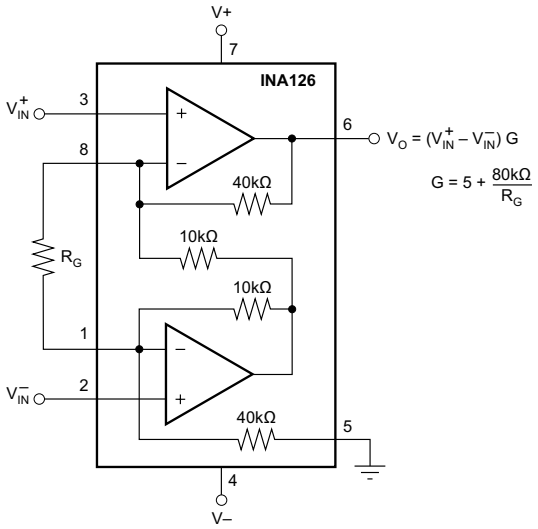
Single version package options include 8-pin plastic PDIP, SOIC-8, and fine-pitch VSSOP-8 surface-mount. Dual version is available in 16-pin plastic PDIP, SOIC-8, and the space-saving, fine-pitch SSOP-16 surface-mount. All are specified for the –40°C to +85°C industrial temperature range.

**Device Information(1)**

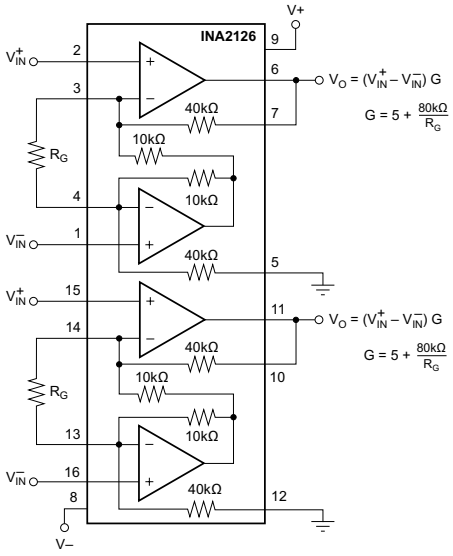
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| INA126 | PDIP (8) | 6.35 mm × 9.81 mm |
| | SOIC (8) | 3.91 mm × 4.90 mm |
| | VSSOP (8) | 3.00 mm × 3.00 mm |
| INA2126 | PDIP (16) | 6.35 mm × 19.30 mm |
| | SOIC (16) | 3.91 mm × 9.90 mm |
| | SSOP (16) | 3.90 mm × 4.90 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic: INA126**




**Simplified Schematic: INA2126**



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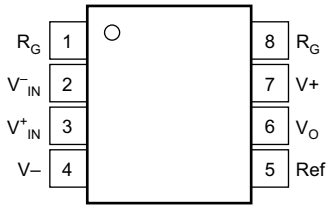
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (August 2005) to Revision B | Page |
|---|---|
| • Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |

# 5 Pin Configuration and Functions

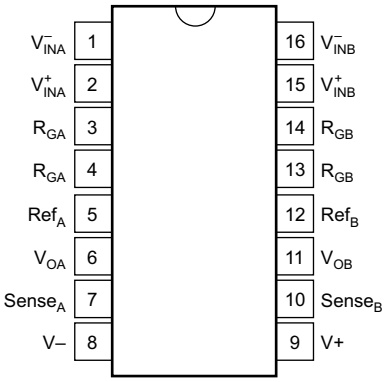
**P, D, and DGK Packages**
**8-Pin PDIP, SOIC, VSSOP**
**Top View**




**Pin Functions: 8-Pin**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1, 8 | $R_G$ | — | Gain setting pin. For gains greater than 5 place a gain resistor between pin 1 and pin 8. |
| 2 | $V-_{IN}$ | I | Negative input |
| 3 | $V+_{IN}$ | I | Positive input |
| 4 | V– | — | Negative supply |
| 5 | Ref | I | Reference input. This pin must be driven by a low impedance or connected to ground. |
| 6 | $V_O$ | O | Output |
| 7 | V+ | — | Positive supply |

**N, D, and DBQ Packages**
**16-Pin PDIP, SOIC, SSOP**
**Top View**




## Pin Functions: 16-Pin

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | $V–_{INA}$ | I | Negative input for amplifier A |
| 2 | $V+_{INA}$ | I | Positive input for amplifier A |
| 3, 4 | $R_{GA}$ | — | Gain setting pin for amplifier A. For gains greater than 5 place a gain resistor between pin 3 and pin 4. |
| 5 | $Ref_A$ | I | Reference input for amplifier A. This pin must be driven by a low impedance or connected to ground. |
| 6 | $V_{OA}$ | O | Output of amplifier A |
| 7 | $Sense_A$ | I | Feedback for amplifier A. Connect to VOA, amplifier A output. |
| 8 | V– | — | Negative supply |
| 9 | V+ | — | Positive supply |
| 10 | $Sense_B$ | I | Feedback for amplifier B. Connect to VOB, amplifier B output. |
| 11 | $V_{OB}$ | O | Output of amplifier B |
| 12 | $Ref_B$ | I | Reference input for amplifier B. This pin must be driven by a low impedance or connected to ground. |
| 13, 14 | $R_{GB}$ | — | Gain setting pin for amplifier B. For gains greater than 5 place a gain resistor between pin 13 and pin 14. |
| 15 | $V+_{INB}$ | I | Positive input for amplifier B |
| 16 | $V–_{INB}$ | I | Negative input for amplifier B |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Power supply voltage, V+ to V– | | 36 | V |
| Input signal voltage (2) | (V–) – 0.7 | (V+) + 0.7 | |
| Input signal current (2) | | 10 | mA |
| Output short circuit | Continuous | | |
| Operating temperature | –55 | 125 | °C |
| Lead temperature (soldering, 10 s) | | 300 | °C |
| Storage temperature, $T_{stg}$ | –55 | 125 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input signal voltage is limited by internal diodes connected to power supplies. See text.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| V+ | V power supply | ±135 | ±15 | ±18 | V |
| $V_O$ | Input common mode voltage for $V_O$ = 0 | | ±11.25 | | V |
| $T_A$ | Operating temperature | –55 | | 125 | °C |

## 6.4 Thermal Information: INA126

| THERMAL METRIC(1) | | INA126 | | | UNIT |
|---|---|---|---|---|---|
| | | PDIP | SOIC | MSOP | |
| | | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 52.2 | 116.4 | 167.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 41.6 | 62.4 | 60.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 29.4 | 57.7 | 88.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 18.9 | 10 | 7.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 29.2 | 57.1 | 87.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | – | – | – | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Thermal Information: INA2126

| THERMAL METRIC(1) | | INA2126 | | | UNIT |
|---|---|---|---|---|---|
| | | PDIP | SOIC | MSOP | |
| | | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 39.3 | 76.2 | 115.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 26.2 | 37.8 | 67 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 20.1 | 33.5 | 58.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 10.7 | 7.5 | 19.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 19.9 | 33.3 | 57.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | – | – | – | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.6 Electrical Characteristics

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_L$ = 25 kΩ ( unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | |
| RTI | Offset voltage | NA126P, U, E; INA2126P, U, E | | | ±100 | ±250 | µV |
| | | INA126PA, UA, EA; INA2126PA, UA, EA | | | ±150 | ±500 | |
| | Offset voltage versus temperature | NA126P, U, E; INA2126P, U, E | | | ±0.5 | ±3 | µV/°C |
| | | INA126PA, UA, EA; INA2126PA, UA, EA | | | ±0.5 | ±5 | |
| | Offset voltage versus power supply (PSRR) | $V_S$ = ±1.35 V to ±18 | VNA126P, U, E INA2126P, U, E | | 5 | 15 | µV/V |
| | | | VINA126PA, UA, EA INA2126PA, UA, EA | | 5 | 50 | |
| | Input impedance | INA126P, U, E; INA2126P, U, E | | | $10^9$ \|\| 4 | | Ω \|\| pF |
| | Safe input voltage | $R_S$ = 0 | | (V–) – 0.5 | | (V+) + 0.5 | V |
| | | $R_S$ = 1 kΩ | | (V–) – 10 | | (V+) + 10 | |
| | Common-mode voltage range | $V_O$ = 0 V | | ±11.25 | ±11.5 | | V |
| | Channel separation (dual) | G = 5, dc | | | 130 | | dB |
| | Common-mode rejection | $R_S$ = 0, $V_{CM}$ = ±11.25 V | INA126P, U, E INA2126P, U, E | 83 | 94 | | dB |
| | | | INA126PA, UA, EA INA2126PA, UA, EA | 74 | 90 | | |
| | | NA2126U (dual SO-16) | | 80 | 94 | | |
| **INPUT BIAS CURRENT** | | | | | | | |
| | Input bias current | INA126P, U, E; INA2126P, U, E | | | –10 | –25 | nA |
| | | INA126PA, UA, EA; INA2126PA, UA, EA | | | | –50 | |
| | Input bias current vs temperature | | | | ±30 | | pA/°C |
| | Offset current | INA126P, U, E; INA2126P, U, E | | | ±0.5 | ±2 | nA |
| | | INA126PA, UA, EA; INA2126PA, UA, EA | | | ±0.5 | ±5 | |
| | Offset current vs temperature | | | | ±10 | | pA/°C |
| **GAIN** | | | | | | | |
| | Gain | | | | G = 5 to 10k | | V/V |
| | Gain equation | | | | G = 5 + 80 kΩ/$R_G$ | | V/V |
| | Gain error | $V_O$ = ±14 V, G = 5 | INA126P, U, E INA2126P, U, E | | ±0.02% | ±0.1% | |
| | | | INA126PA, UA, EA INA2126PA, UA, EA | | ±0.02% | ±0.18% | |
| | Gain error vs temperature | G = 5 | | | ±2 | ±10 | ppm/°C |
| | Gain error | $V_O$ = ±12 V, G = 100 | INA126P, U, E INA2126P, U, E | | ±0.2% | ±0.5% | |
| | | | INA126PA, UA, EA INA2126PA, UA, EA | | ±0.2% | ±1% | |
| | Gain error vs temperature | G = 100 | | | ±25 | ±100 | ppm/°C |

## Electrical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_L$ = 25 kΩ ( unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Nonlinearity | G = 100, $V_O$ = ±14 V | | ±0.002% | ±0.012% | |
| **NOISE** | | | | | |
| Voltage noise | f = 1 kHz | | 35 | | nV/√Hz |
| | f = 100 Hz | | 35 | | |
| | f = 10 Hz | | 45 | | |
| | $f_B$ = 0.1 Hz to 10 Hz | | 0.7 | | $\mu V_{PP}$ |
| Current noise | f = 1 kHz | | 60 | | fA/√Hz |
| | $f_B$ = 0.1 Hz to 10 Hz | | 2 | | $pA_{PP}$ |
| **OUTPUT** | | | | | |
| Positive voltage | $R_L$ = 25 kΩ | (V+) – 0.9 | (V+) – 0.75 | | V |
| Negative voltage | $R_L$ = 25 kΩ | (V–) + 0.95 | (V–) + 0.8 | | |
| Short-circuit current | Short circuit to ground | | +10 / –5 | | mA |
| Capacitive load drive | | | 1000 | | pF |
| **FREQUENCY RESPONSE** | | | | | |
| Bandwidth, –3dB | G = 5 | | 200 | | kHz |
| | G = 100 | | 9 | | |
| | G = 500 | | 1.8 | | |
| Slew rate | $V_O$ = ±10 V, G = 5 | | 0.4 | | V/µs |
| Settling time, 0.01% | 10-V step, G = 5 | | 30 | | µs |
| | 10-V step, G = 100 | | 160 | | |
| | 10-V step, G = 500 | | 1500 | | |
| Overload recovery | 50% input overload | | 4 | | µs |
| **POWER SUPPLY** | | | | | |
| Voltage range | | ±1.35 | ±15 | ±18 | V |
| Current (per channel) | $I_O$ = 0 | | ±175 | ±200 | µA |
| Specification temperature range | | –40 | | 85 | °C |
| Operation temperature range | | –55 | | 125 | °C |

## 6.7 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = ±15 V (unless otherwise noted)

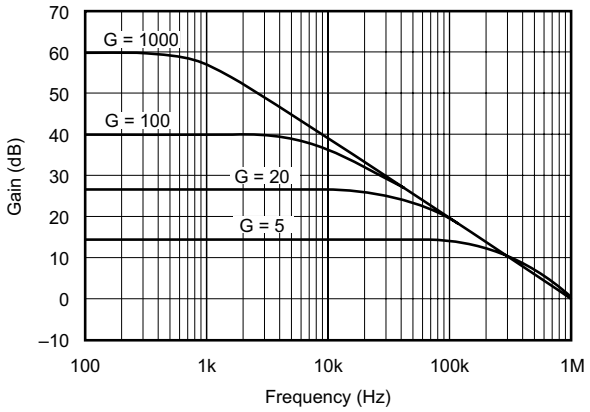



**Figure 1. Gain vs Frequency**

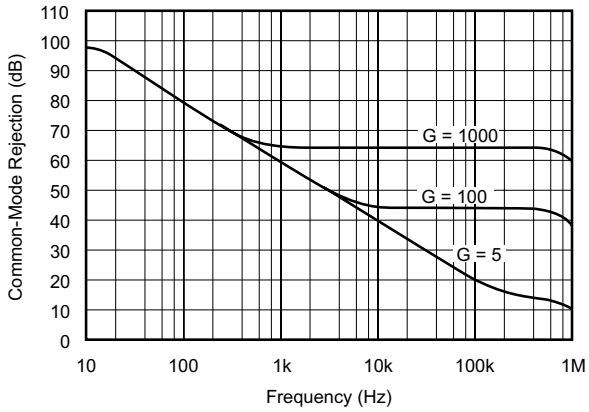



**Figure 2. Common-Mode Rejection vs Frequency**

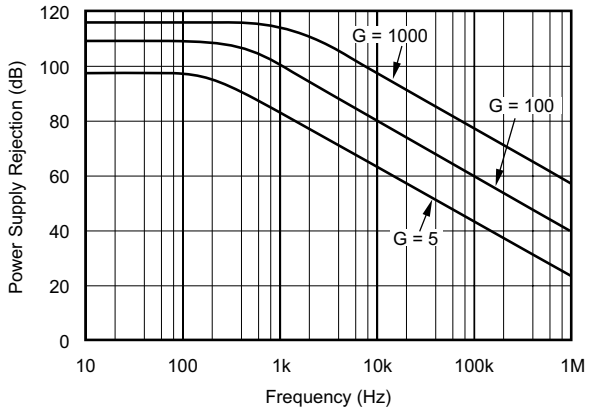



**Figure 3. Positive Power Supply Rejection vs Frequency**

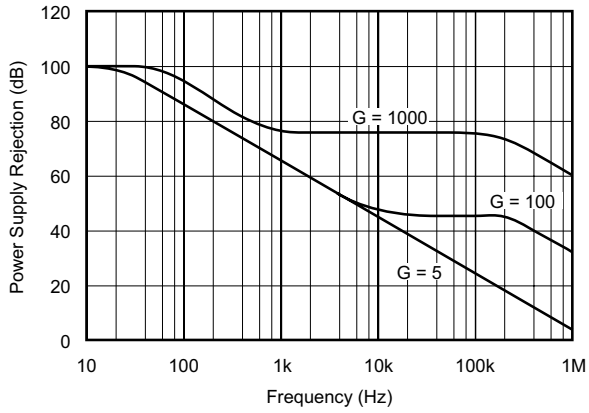



**Figure 4. Negative Power Supply Rejection vs Frequency**

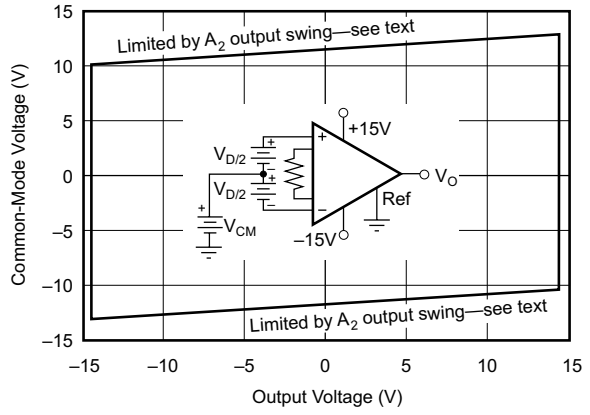



**Figure 5. Input Common-Mode Range vs Output Voltage, $V_S$ = ±15 V**

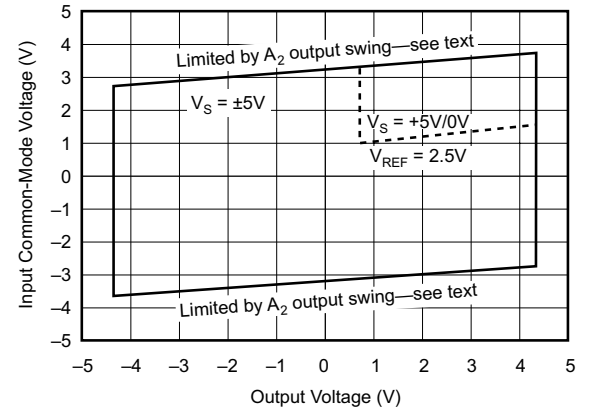



**Figure 6. Input Common-Mode Voltage Range vs Output Voltage, $V_S$ = ±5 V**

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V (unless otherwise noted)

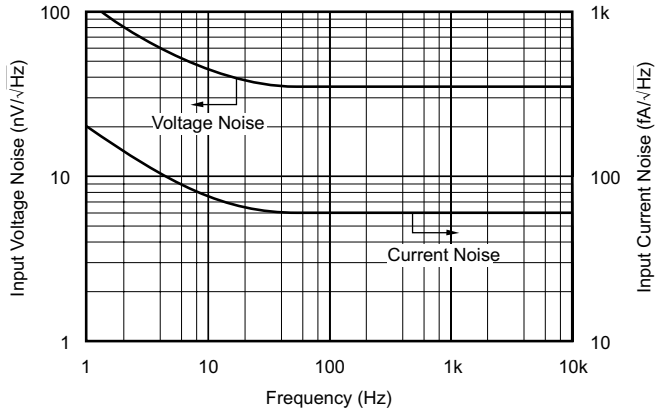



**Figure 7. Input-Referred Noise vs Frequency**

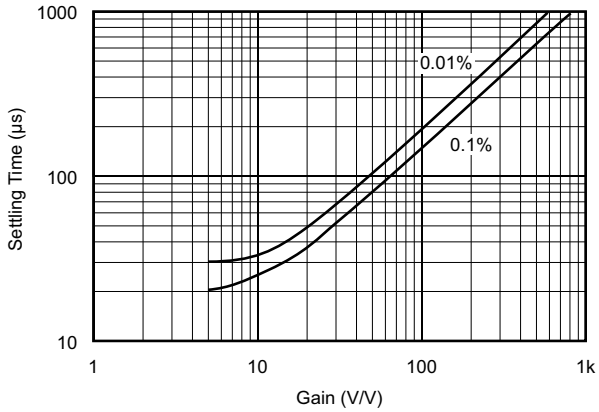



**Figure 8. Settling Time vs Gain**

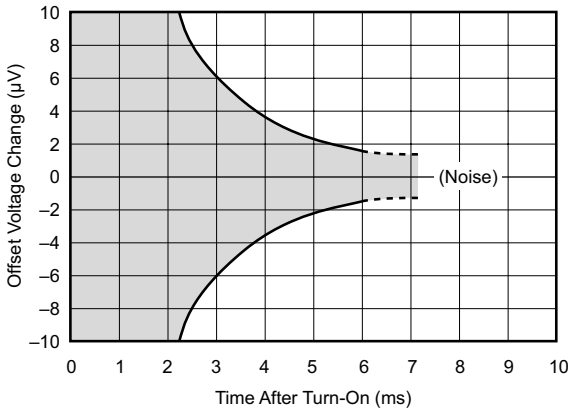



**Figure 9. Input-Referred Offset Voltage Warm-Up**

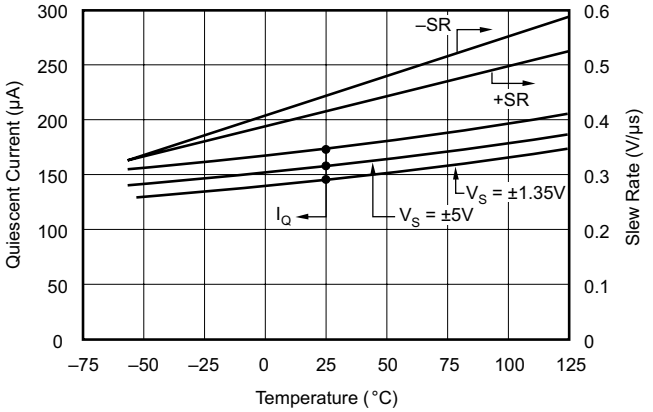



**Figure 10. Quiescent Current and Slew Rate vs Temperature**

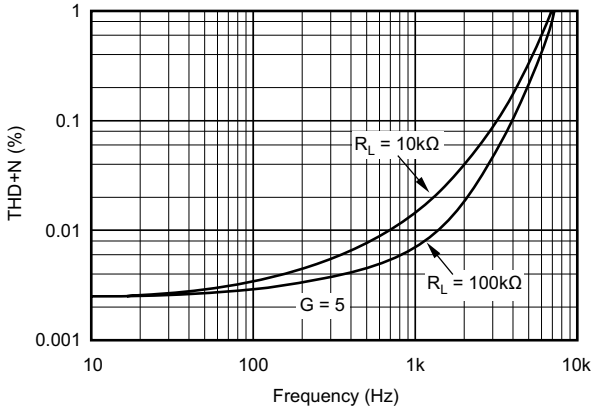



**Figure 11. Total Harmonic Distortion + Noise vs Frequency**

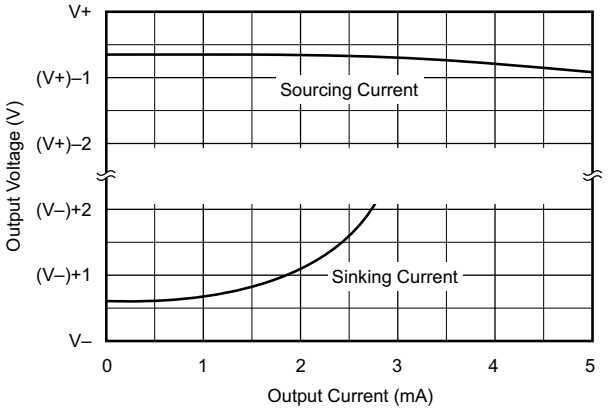



**Figure 12. Output Voltage Swing vs Output Current**

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V (unless otherwise noted)

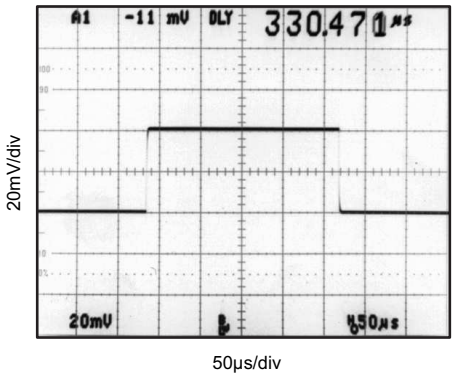



**Figure 13. Small-Signal Response, G = 5**

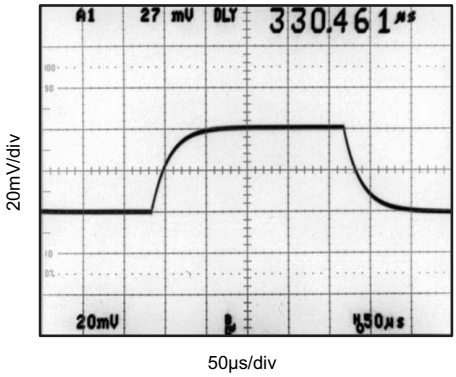



**Figure 14. Small-Signal Response, G = 100**

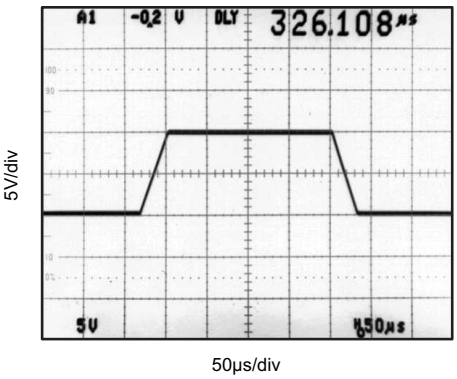



**Figure 15. Large-Signal Response, G = 5**

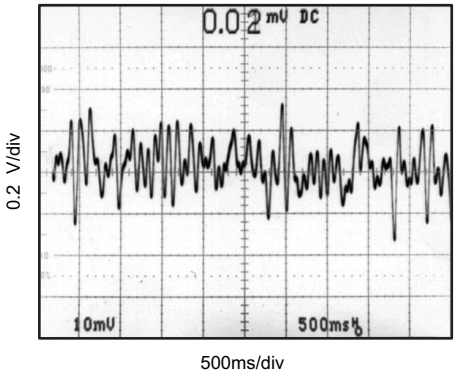



**Figure 16. Voltage Noise, 0.1 Hz to 10 Hz**

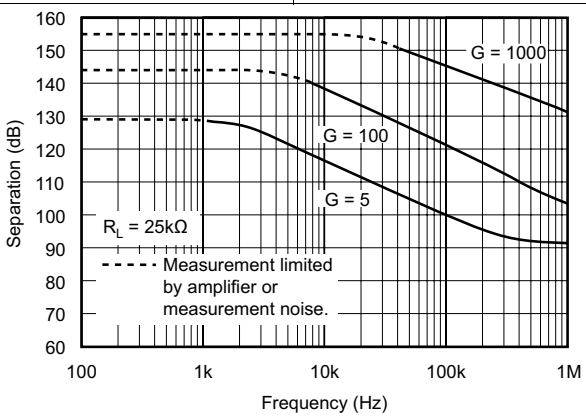



**Figure 17. Channel Separation vs Frequency, RTI (Dual Version)**

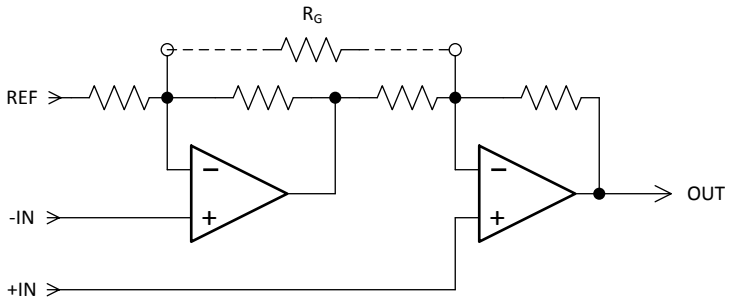
# 7 Detailed Description

## 7.1 Overview

The INAx126 use only two, rather than three, operational amplifiers providing savings in power consumption. In addition the input resistance is high and balanced, thus permitting the signal source to have an unbalanced output impedance.

A minimum circuit gain of 5 permits an adequate DC common mode input range, as well as sufficient bandwidth for most applications.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

The INAx126 are low power, general-purpose instrumentation amplifiers offering excellent accuracy. The versatile two-operational-amplifier design and small size make the amplifiers ideal for a wide range of applications. The two op amp topology reduces power consumption. A single external resistor sets any gain from 5 to 10,000. These devices operate with power supplies as low as ±1.35 V, and quiescent current of 200 µA maximum.

## 7.4 Device Functional Modes

### 7.4.1 Single-Supply Operation

The INAx126 can be used on single power supplies of 2.7 V to 36 V. Use the output REF pin to level shift the internal output voltage into a linear operating condition. Ideally, connecting the REF pin to a potential that is midsupply avoids saturating the output of the amplifiers. See *Application Information* for information on how to adequately drive the reference pin.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The INAx126 measures small differential voltage with high common-mode voltage developed between the noninverting and inverting input. The high input impedance make the INAx126 suitable for a wide range of applications. The INAx126 can adjust the functionality of the output signals by setting the reference pin, giving additional flexibility that is practical for multiple configurations.

## 8.2 Typical Application

Figure 18 shows the basic connections required for operation of the INA126. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal, which is normally grounded. This connection must be low-impedance to ensure good common-mode rejection. A resistance of 8 Ω in series with the Ref pin causes a typical device to degrade to approximately 80-dB CMR.

Figure 18 depicts a desired differential signal from a sensor at 1kHz and 5mV p-p superimposed on top of a 1-V p-p 60-Hz common mode signal (the 1-kHz signal can not be resolved in this scope trace). The FFT trace in Figure 22 shows the two signals. Figure 23 shows the clearly recovered differential signal at the output of the INA126 operating at a gain of 250. The FFT of figure 4 shows the 60-Hz common-mode is no longer visible.

The dual version (INA2126) has feedback-sense connections, $Sense_A$ and $Sense_B$. These must be connected to their respective output terminals for proper operation. The sense connection can sense the output voltage directly at the load for best accuracy.

| DESIRED GAIN (V/V) | $R_G$ (Ω) | NEAREST 1% $R_G$ VALUE |
|---|---|---|
| 5 | NC | NC |
| 10 | 16k | 15.8k |
| 20 | 5333 | 5360 |
| 50 | 1779 | 1780 |
| 100 | 842 | 845 |
| 200 | 410 | 412 |
| 500 | 162 | 162 |
| 1000 | 80.4 | 80.6 |
| 2000 | 40.1 | 40.2 |
| 5000 | 16.0 | 15.8 |
| 10000 | 8.0 | 7.87 |

NC: No Connection.

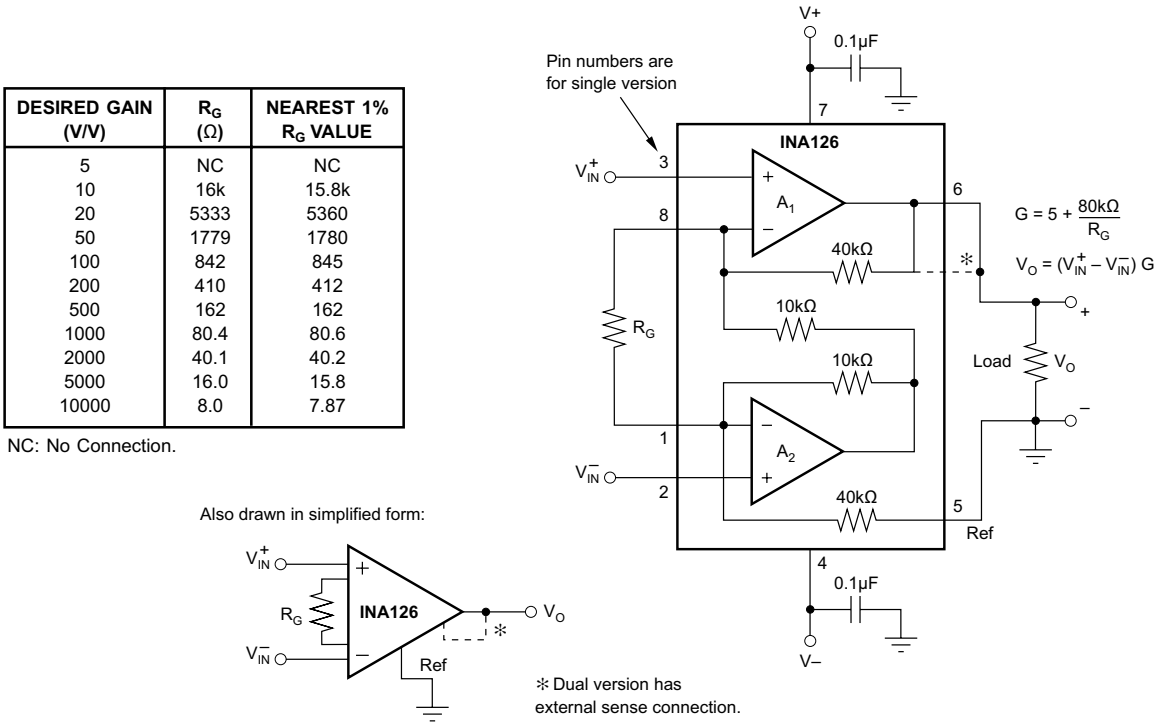



**Figure 18. Basic Connections**

## Typical Application (continued)

### 8.2.1 Design Requirements

For the traces shown in Figure 19 and Figure 20:

- Common-mode rejection of at least 80dB
- Gain of 250

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Setting the Gain*

Gain is set by connecting an external resistor, $R_G$:

$$g = 5 + 80\ k\Omega/R_G \quad (1)$$

Commonly used gains and $R_G$ resistor values are shown in Figure 18.

The 80-kΩ term in Equation 1 comes from the internal metal film resistors, which are laser-trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications.

The stability and temperature drift of the external gain setting resistor, $R_G$, also affects gain. The $R_G$ contribution to gain accuracy and drift can be directly inferred from Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error in gains of approximately 100 or greater.

#### *8.2.2.2 Offset Trimming*

The INAx126 are laser-trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 19 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref terminal is added to the output signal. An operational amplifier buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

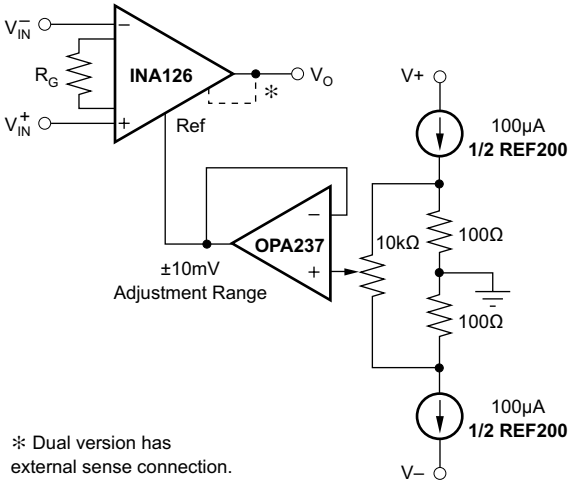



**Figure 19. Optional Trimming of Output Offset Voltage**

## Typical Application (continued)

### 8.2.2.3 Input Bias Current Return

The input impedance of the INAx126 is extremely high, approximately 109 Ω. However, a path must be provided for the input bias current of both inputs. This input bias current is typically –10 nA (current flows out of the input terminals). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 20 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range, and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 20). With higher source impedance, using two equal resistors provides a balanced input with the advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

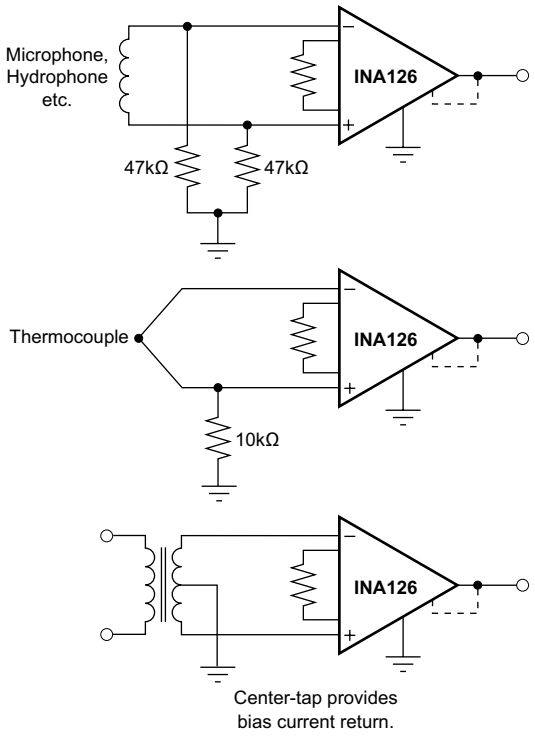



**Figure 20. Providing an Input Common-Mode Current Path**

### 8.2.2.4 Input Common-Mode Range

The input common-mode range of the INAx126 is shown in *Typical Characteristics*. The common-mode range is limited on the negative side by the output voltage swing of $A_2$, an internal circuit node that cannot be measured on an external pin. The output voltage of $A_2$ can be expressed as shown in Equation 2:

$$V_{O2} = 1.25\ V^-_{IN} - (V^+_{IN} - V^-_{IN})\ (10\ k\Omega/R_G) \quad (2)$$

where

- Voltages referred to Ref terminal, pin 5

The internal op amp $A_2$ is identical to $A_1$, and its output swing is limited to typically 0.7 V from the supply rails. When the input common-mode range is exceeded ($A_2$ output is saturated), $A_1$ can still be in linear operation and respond to changes in the non-inverting input voltage. The output voltage, however, will be invalid.

## Typical Application (continued)

### 8.2.2.5 Input Protection

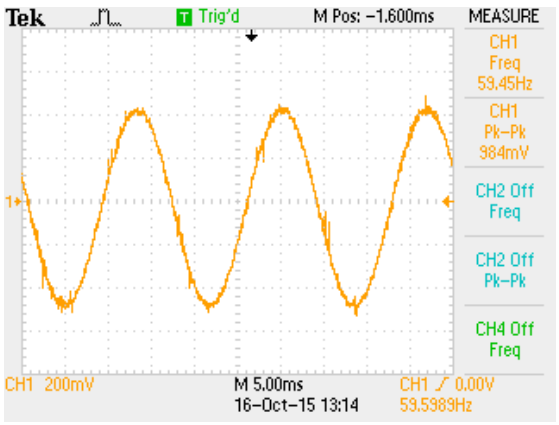
The inputs are protected with internal diodes connected to the power supply rails. These diodes clamp the applied signal to prevent it from exceeding the power supplies by more than approximately 0.7 V. If the signal-source voltage can exceed the power supplies, the source current should be limited to less than 10 mA. This can generally be done with a series resistor. Some signal sources are inherently current-limited, and do not require limiting resistors.

### 8.2.2.6 Channel Crosstalk—Dual Version

The two channels of the INA2126 are completely independent, including all bias circuitry. At DC and low frequency, there is virtually no signal coupling between channels. Crosstalk increases with frequency and is dependent on circuit gain, source impedance, and signal characteristics.

As source impedance increases, careful circuit layout can help achieve lowest channel crosstalk. Most crosstalk is produced by capacitive coupling of signals from one channel to the input section of the other channel. To minimize coupling, separate the input traces as far as practical from any signals associated with the opposite channel. A grounded guard trace surrounding the inputs helps reduce stray coupling between channels. Carefully balance the stray capacitance of each input to ground, and run the differential inputs of each channel parallel to each other, or directly adjacent on top and bottom side of a circuit board. Stray coupling then tends to produce a common-mode signal that is rejected by the IA input.

### 8.2.3 Application Curves




Differential signal is too small to be seen

**Figure 21. Common-mode Signal at INA126 Input**

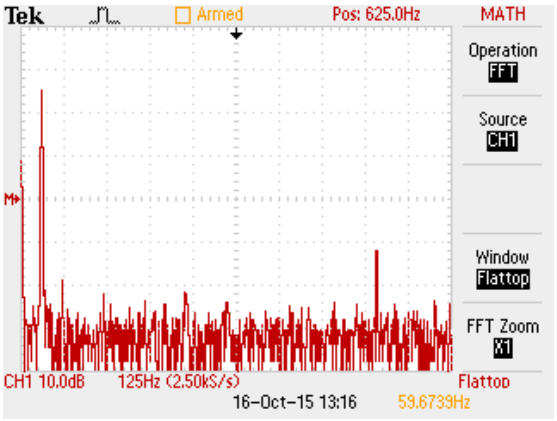



**Figure 22. FFT of Signal in Figure 21 Shows Both the 60-Hz Common-mode Along With 5-kHz Differential Signal**

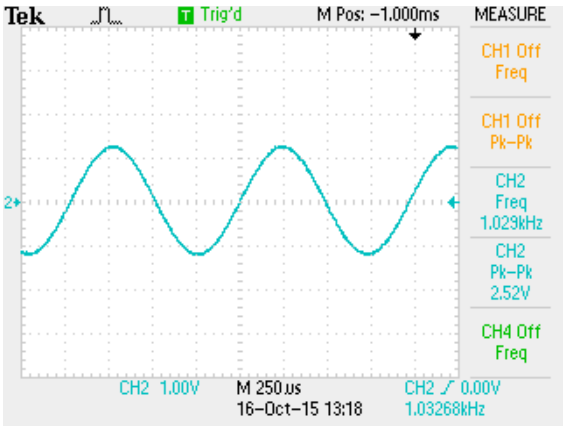



**Figure 23. Recovered Differential Signal at the Output of the INA126 With a Gain of 250**

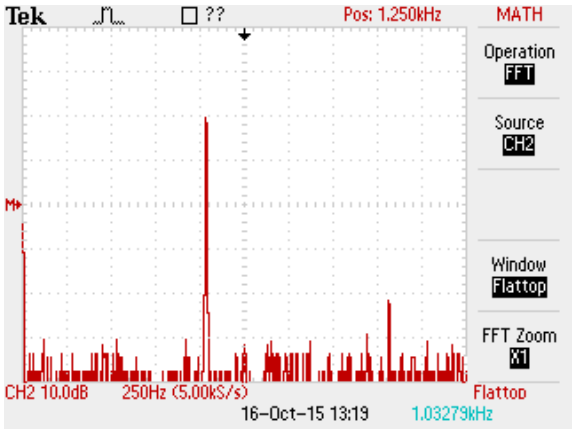



**Figure 24. FFT of the INA126 Output Shows that the 60-Hz Common-mode Signal is Rejected**

# 9 Power Supply Recommendations

## 9.1 Low Voltage Operation

The INAx126 can be operated on power supplies as low as ±1.35 V. Performance remains excellent with power supplies ranging from ±1.35 V to ±18 V. Most parameters vary only slightly throughout this supply voltage range (see *Typical Characteristics*). Operation at low supply voltage requires careful attention to ensure that the common-mode voltage remains within its linear range (see Figure 5 and Figure 6).

The INAx126 can be operated from a single power supply with careful attention to input common-mode range, output voltage swing of both op amps, and the voltage applied to the Ref terminal. Figure 25 shows a bridge amplifier circuit operated from a single +5-V power supply. The bridge provides an input common-mode voltage near 2.5 V, with a relatively small differential voltage.

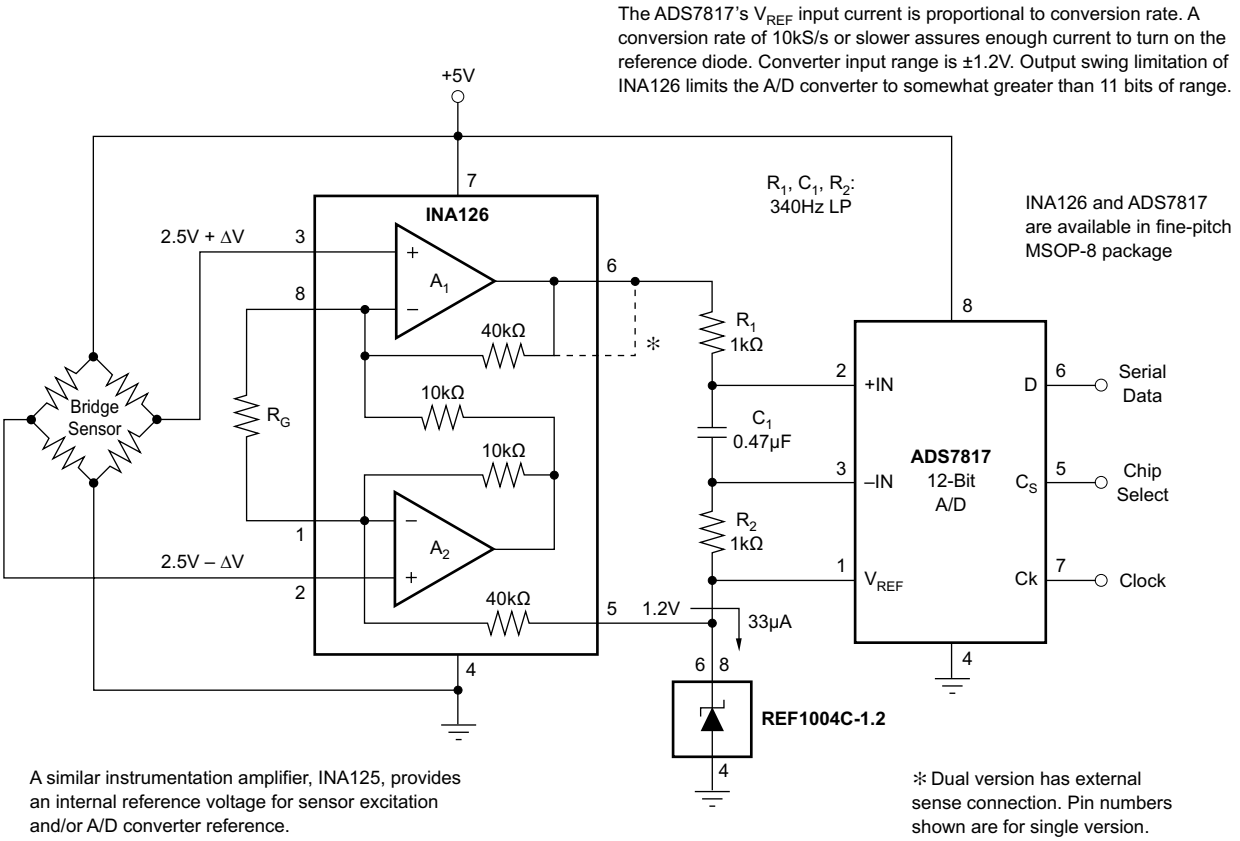



**Figure 25. Bridge Signal Acquisition, Single 5-V Supply**

# 10 Layout

## 10.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Take care to ensure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of RG, select the component so that the switch capacitance is as small as possible.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see SLOA089, Circuit Board Layout Techniques.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 26, keeping RG close to the pins minimizes parasitic capacitance.
- Keep the traces as short as possible

## 10.2 Layout Example

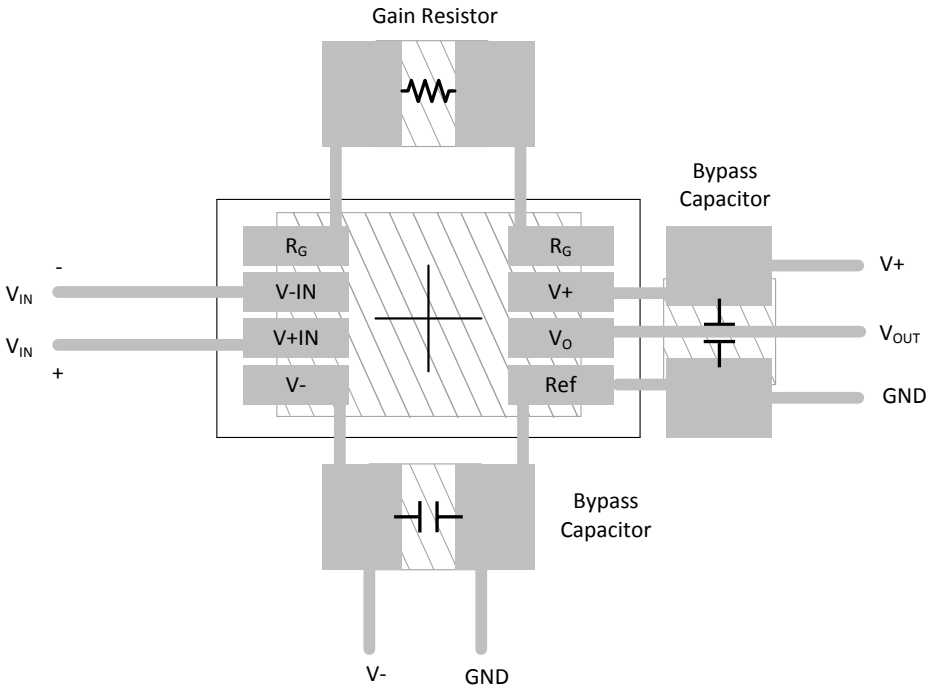



**Figure 26. Layout for All Single INA126 Versions**

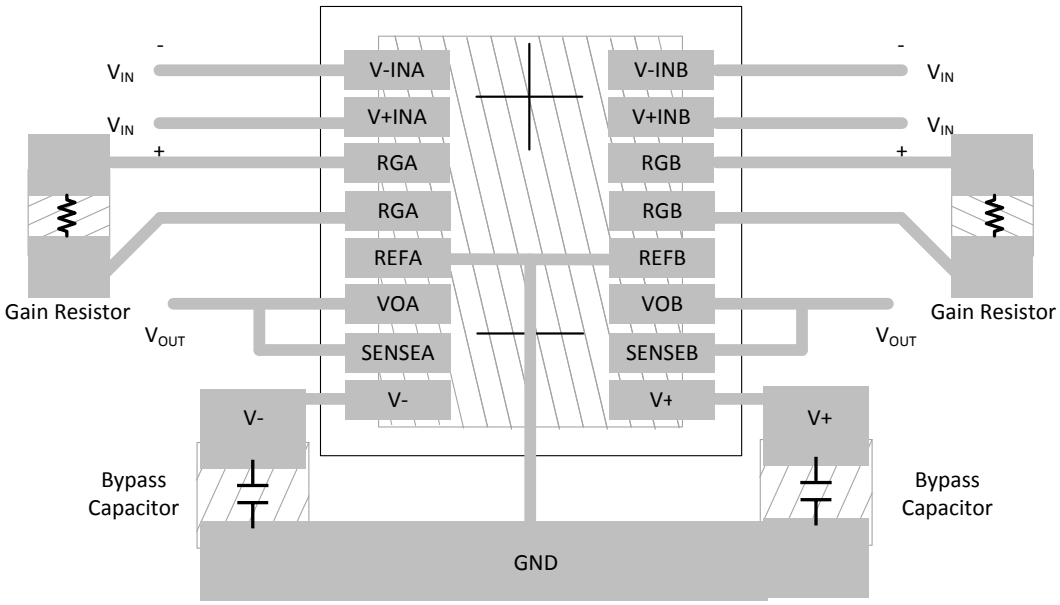



**Figure 27. INA2126 Layout**

# 11 Device and Documentation Support

## 11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| INA126 | Click here | Click here | Click here | Click here | Click here |
| INA2126 | Click here | Click here | Click here | Click here | Click here |

## 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| INA126E/250 | ACTIVE | VSSOP | DGK | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-2-260C-1 YEAR | -55 to 125 | A26 | Samples |
| INA126E/250G4 | ACTIVE | VSSOP | DGK | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -55 to 125 | A26 | Samples |
| INA126E/2K5 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-2-260C-1 YEAR | | A26 | Samples |
| INA126E/2K5G4 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | | A26 | Samples |
| INA126EA/250 | ACTIVE | VSSOP | DGK | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-2-260C-1 YEAR | | A26 | Samples |
| INA126EA/2K5 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-2-260C-1 YEAR | | A26 | Samples |
| INA126EA/2K5G4 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | | A26 | Samples |
| INA126P | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | | INA126P | Samples |
| INA126PA | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | | INA126P A | Samples |
| INA126U | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | INA 126U | Samples |
| INA126U/2K5 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | INA 126U | Samples |
| INA126U/2K5G4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | INA 126U | Samples |
| INA126UA | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | INA 126U A | Samples |
| INA126UA/2K5 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | INA 126U A | Samples |
| INA126UAG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | INA 126U A | Samples |
| INA2126E/250 | ACTIVE | SSOP | DBQ | 16 | 250 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | | INA 2126E | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | A | |
| INA2126E/250G4 | ACTIVE | SSOP | DBQ | 16 | 250 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | | INA 2126E A | Samples |
| INA2126E/2K5 | ACTIVE | SSOP | DBQ | 16 | 2500 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | | INA 2126E A | Samples |
| INA2126EA/250 | ACTIVE | SSOP | DBQ | 16 | 250 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | | INA 2126E A | Samples |
| INA2126EA/250G4 | ACTIVE | SSOP | DBQ | 16 | 250 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | | INA 2126E A | Samples |
| INA2126EA/2K5 | ACTIVE | SSOP | DBQ | 16 | 2500 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | | INA 2126E A | Samples |
| INA2126U | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | INA2126U | Samples |
| INA2126UA | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | INA2126U A | Samples |
| INA2126UA/2K5 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | INA2126U A | Samples |
| INA2126UE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | INA2126U | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

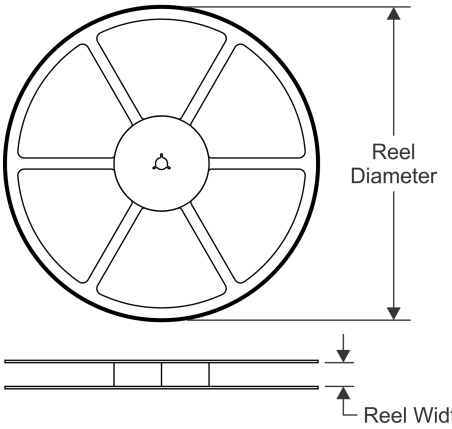
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

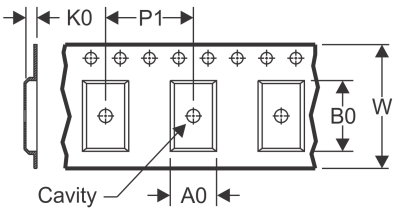
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

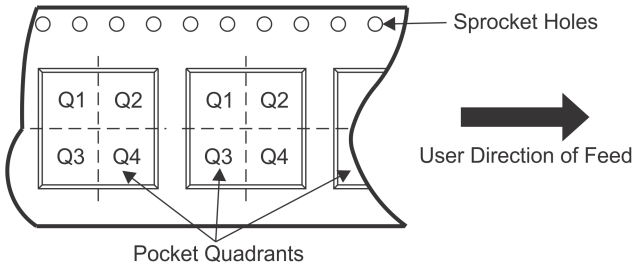



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

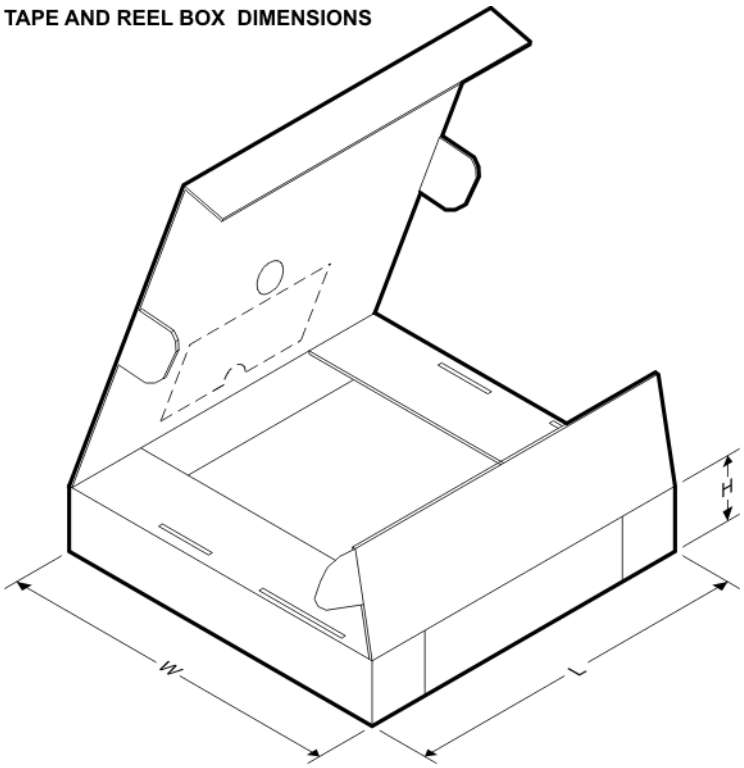
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INA126E/250 | VSSOP | DGK | 8 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA126E/2K5 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA126EA/250 | VSSOP | DGK | 8 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA126EA/2K5 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA126U/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| INA126UA/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| INA2126UA/2K5 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

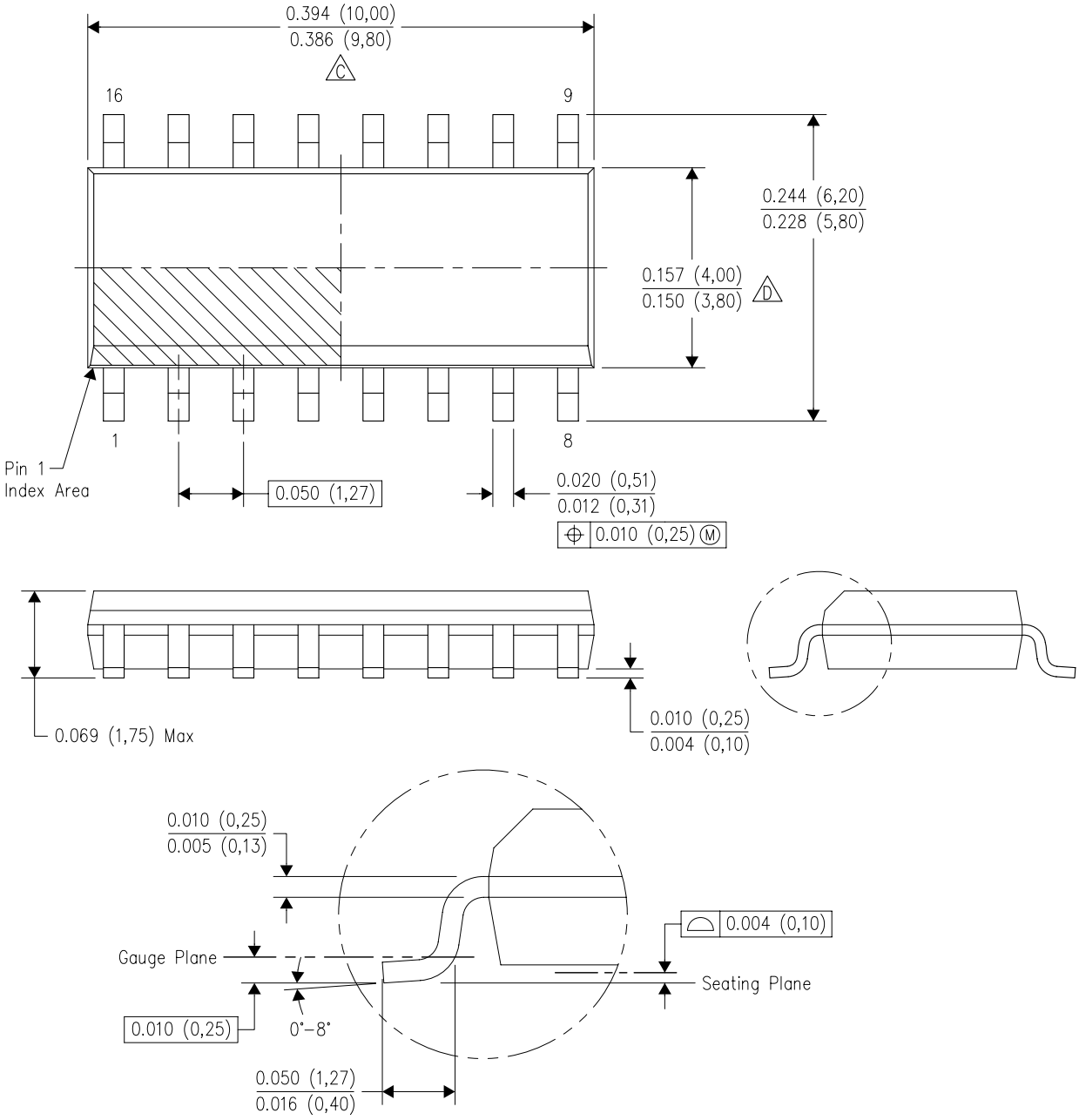
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

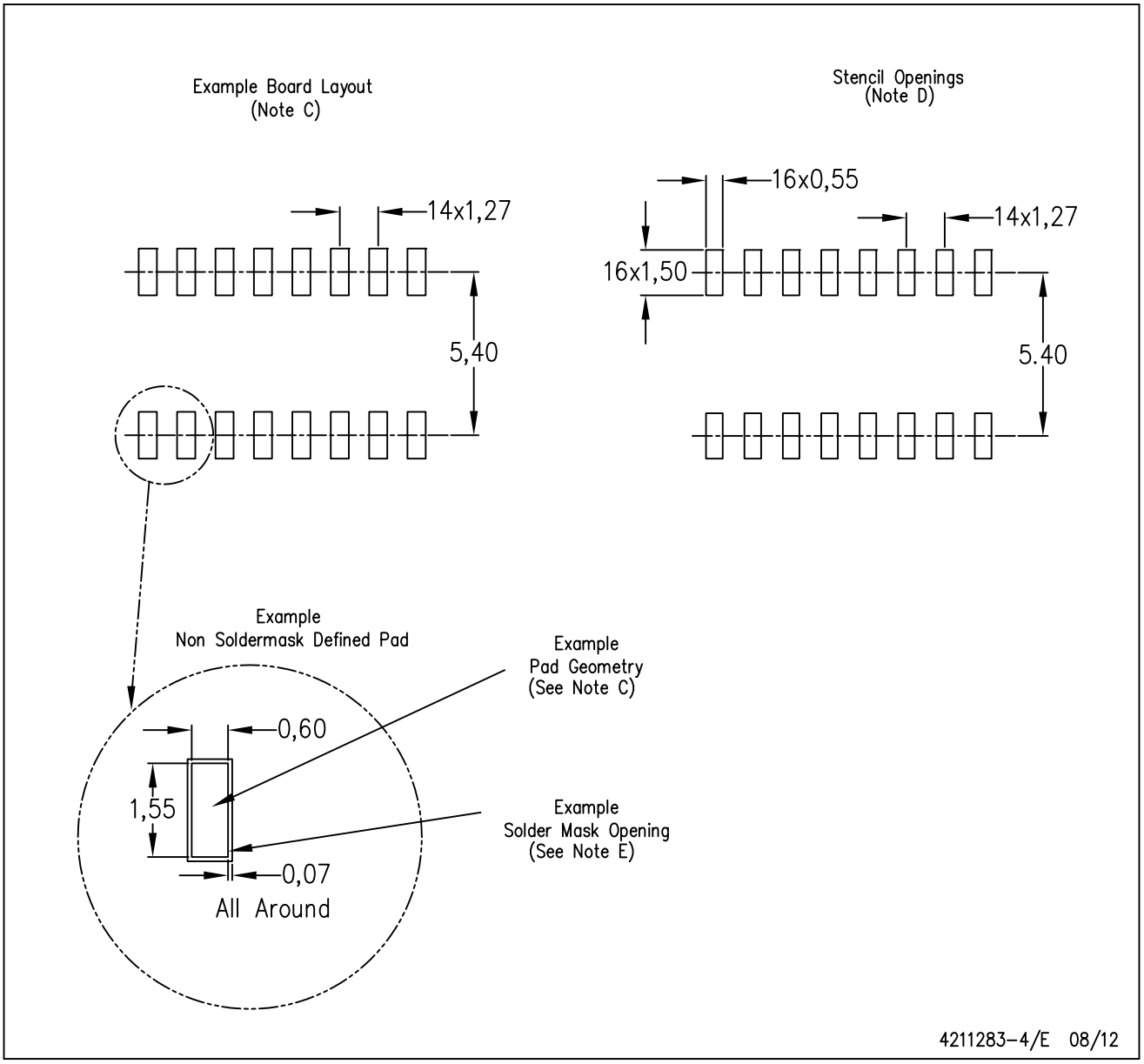
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| INA126E/250 | VSSOP | DGK | 8 | 250 | 210.0 | 185.0 | 35.0 |
| INA126E/2K5 | VSSOP | DGK | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| INA126EA/250 | VSSOP | DGK | 8 | 250 | 210.0 | 185.0 | 35.0 |
| INA126EA/2K5 | VSSOP | DGK | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| INA126U/2K5 | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| INA126UA/2K5 | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| INA2126UA/2K5 | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



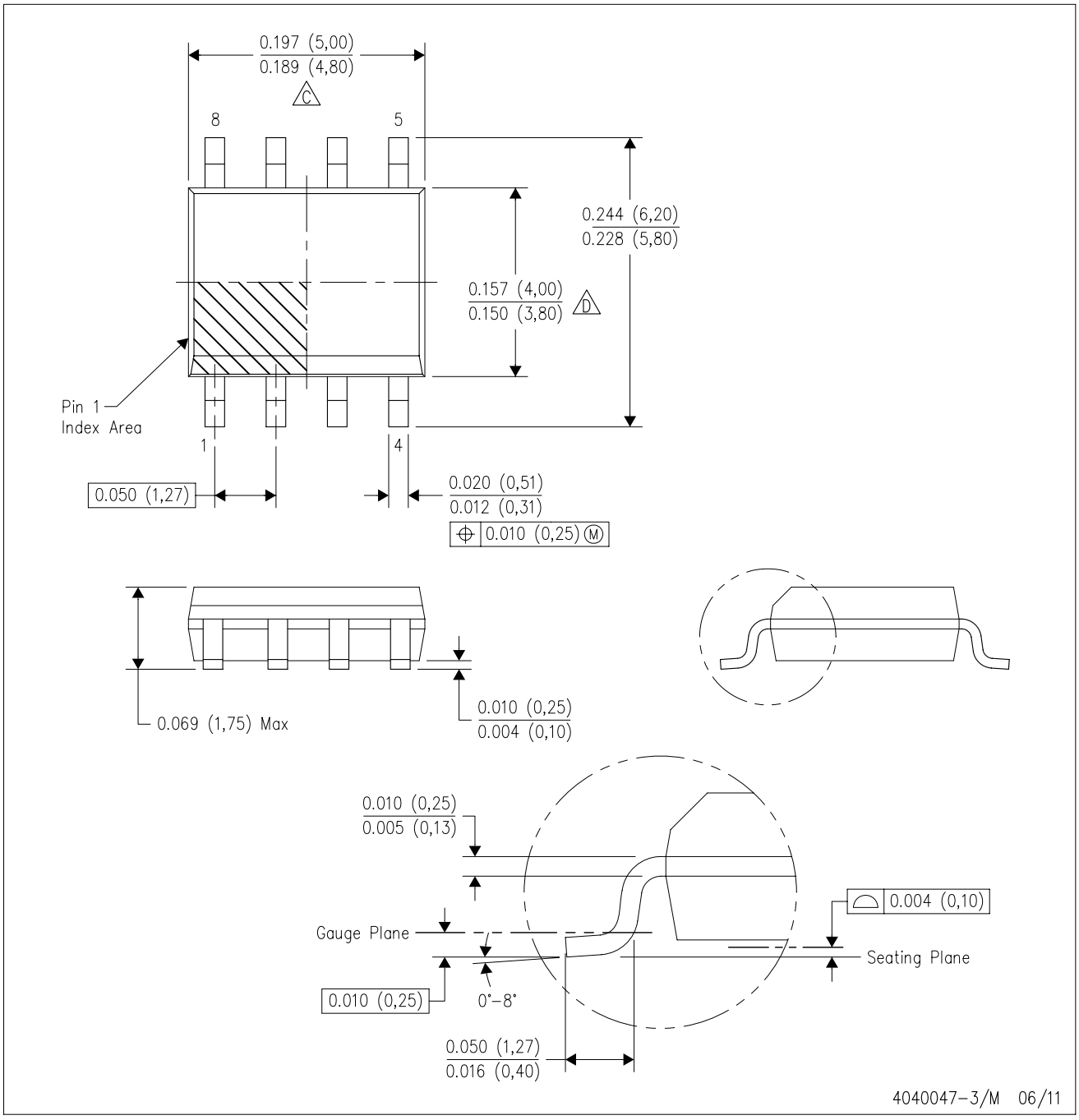

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



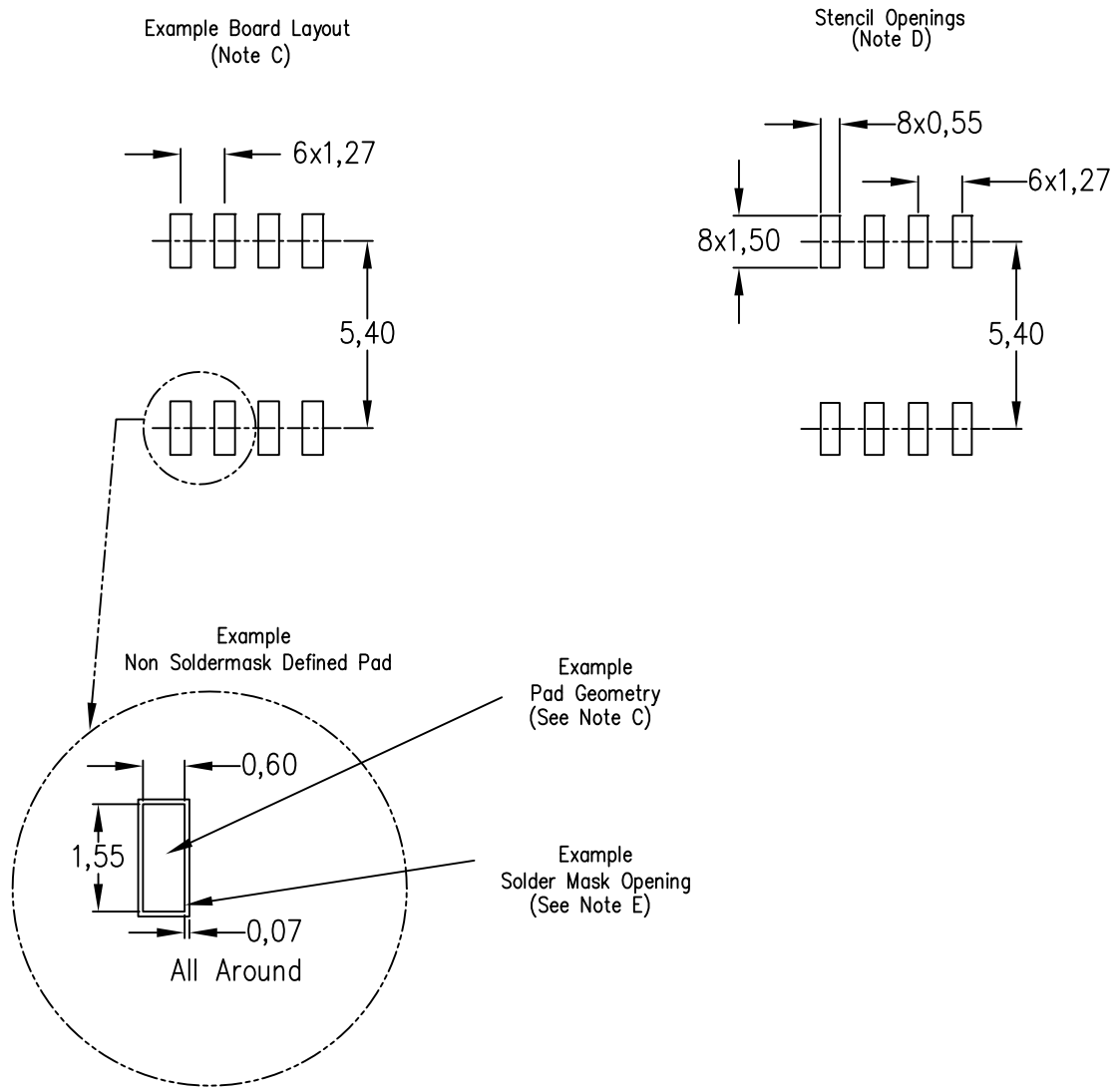

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE

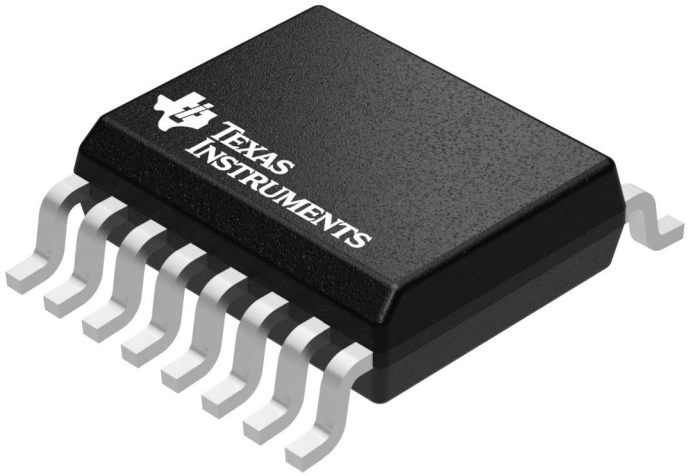



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# GENERIC PACKAGE VIEW

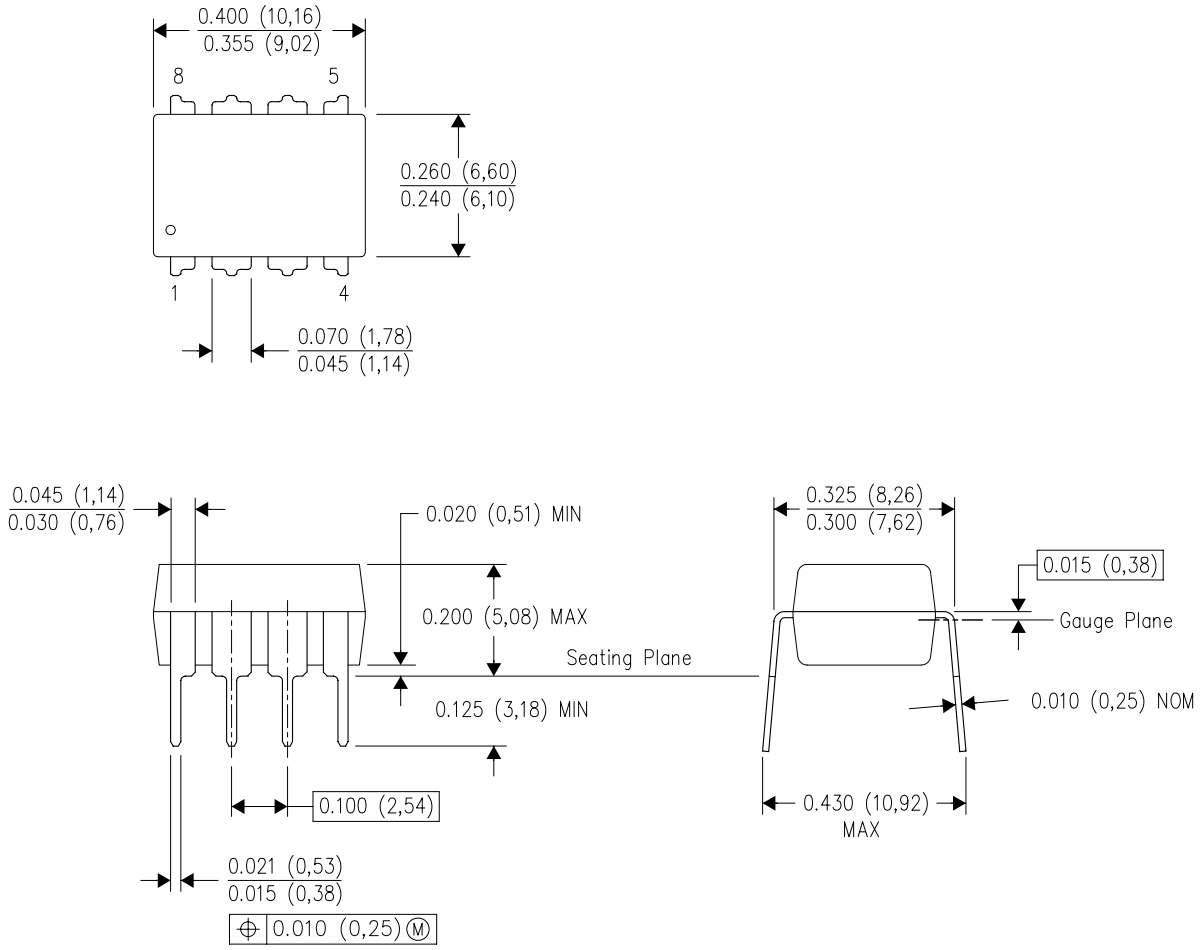
## DBQ 16 SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



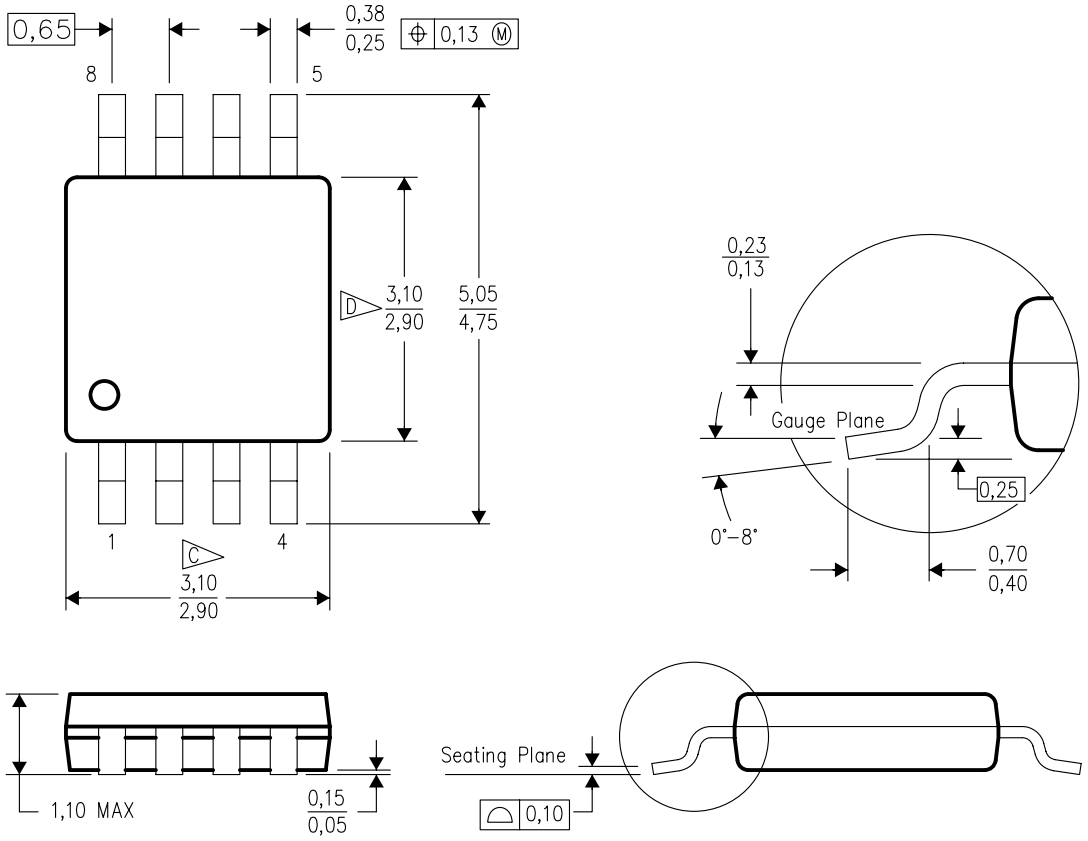

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

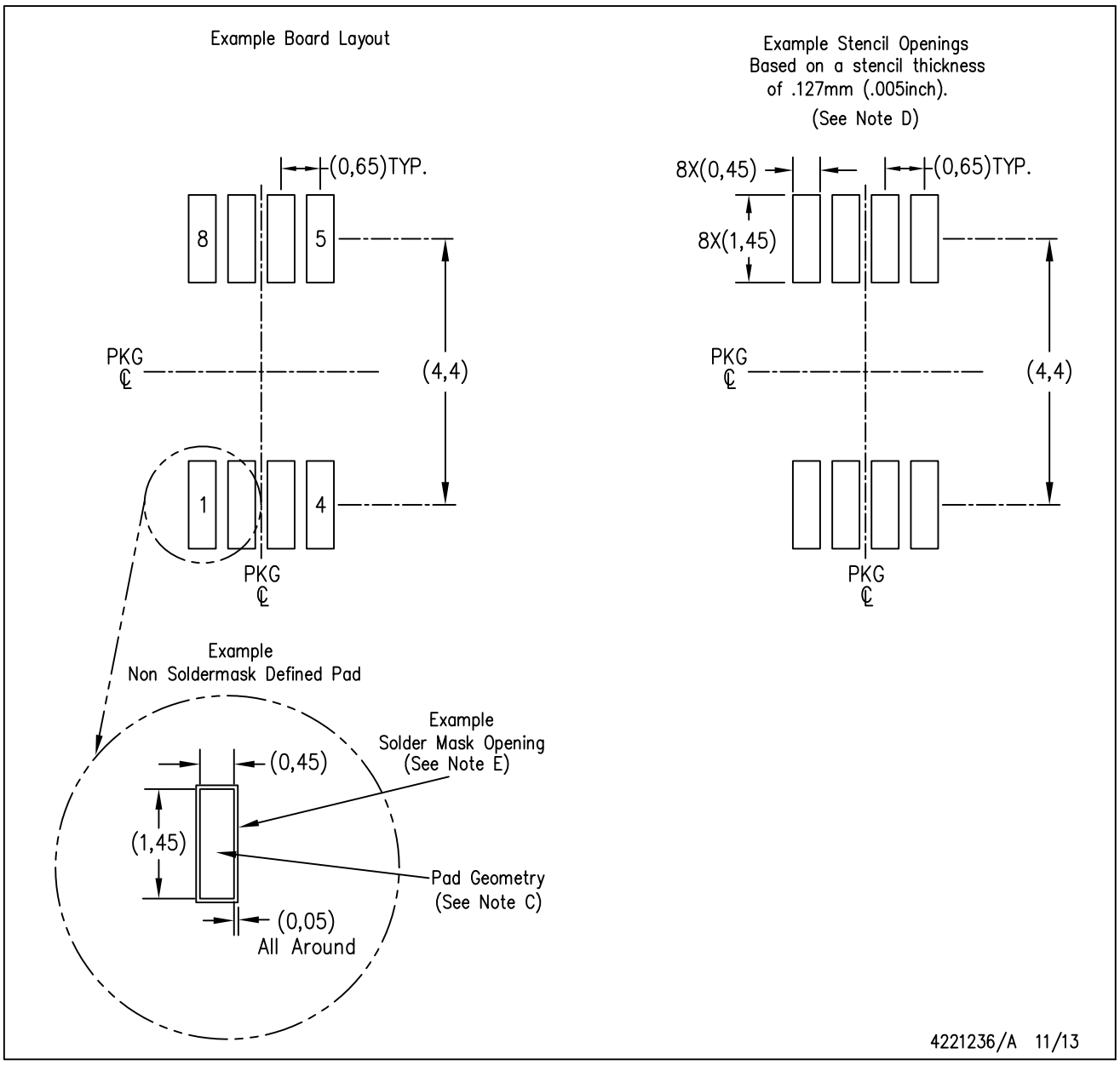
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

# DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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