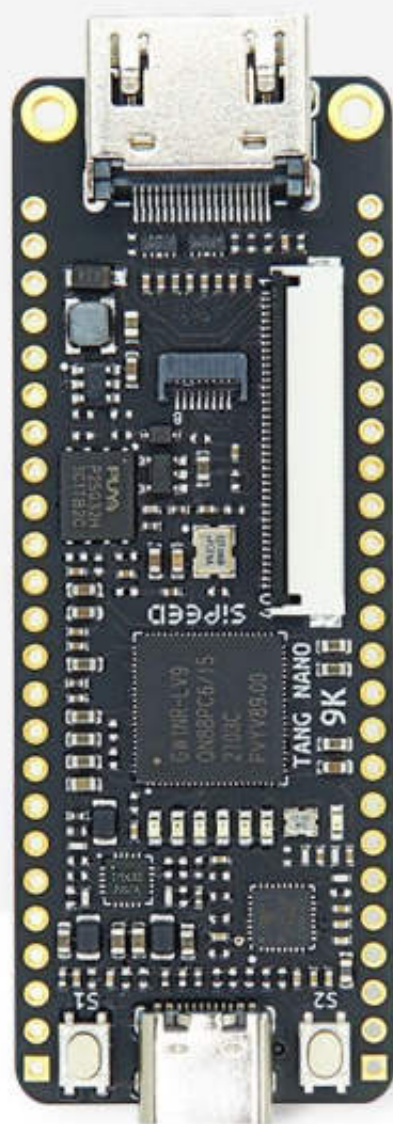


SIPEED TANG NANO 9K

ENTRY-LEVEL FPGA KIT FOR RISC-V



RISC-V Soft Core
Experiment



PicoRV
Is Available



Support Multiple
Display Interfaces



Compatible
Bread Board

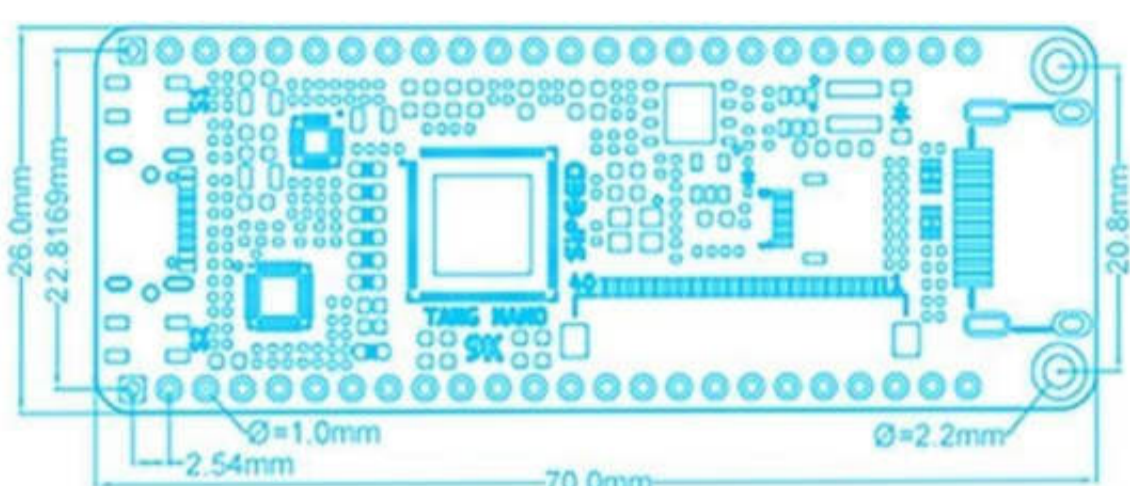
Characteristic

Logical Unit (LUT4)	8640
Flip - Flop (FF)	6480
Shadow SRAM SSRAM (bits)	17280
Block SRAM BSRAM	468K
BSRAM Quantity BSRAM	26
User Flash (bits)	608K
PSRAM (bits)	64M
High Performance DSP	Support 9x9,18x18,36x36bits multiplier and 54bits accumulator
18 x 18 Multiplier	20
SPI FLASH	32M-bit
PLLs	2
Display Interface	Screen connector, RGB interface connector, SPI interface connector
Debugger	Onboard BL702, which provides USB-JTAG and USB-UART for GW1NR-9
IO	<ul style="list-style-type: none">• Support 4mA, 8mA, 16mA, 24mA and other driving capabilities• Independent bus keeper, pull-up / pull-down resistor and open drain output options are provided for each I/O
Connector	TF card slot , 2x24P 2.54mm IO pad
Button	Onboard 2 user buttons
LED	Onboard 6 LEDs

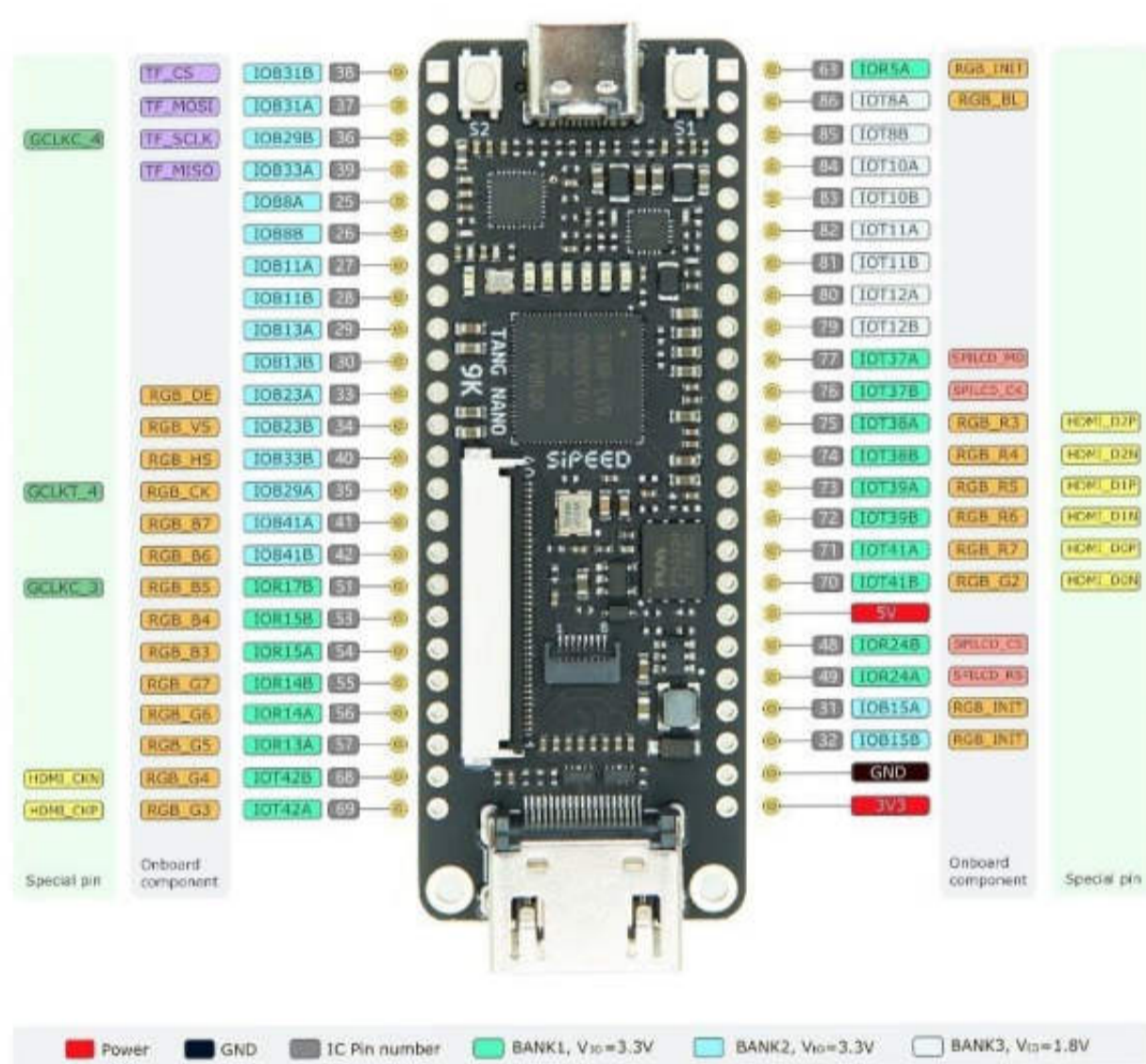
Function Annotation



— ANNOTATION —

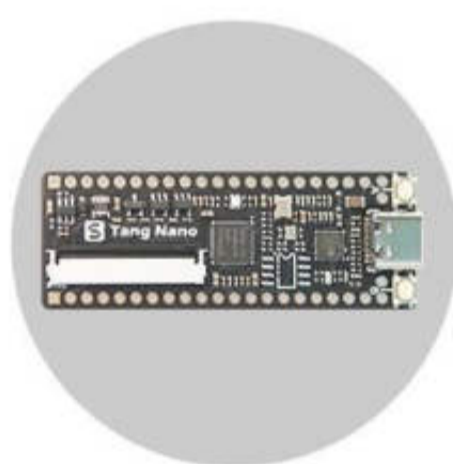


— DIMENSION —

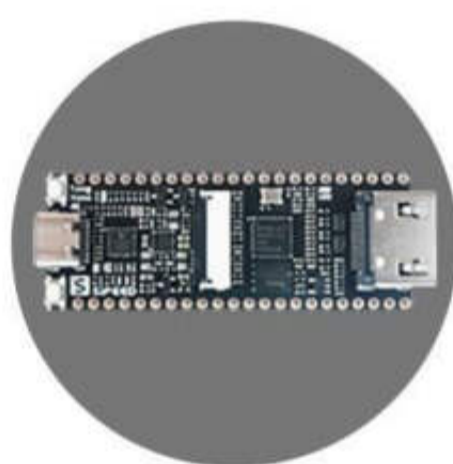


— PINS —

Contrast



Tang Nano 1K



Tang Nano 4K



Tang Nano 9K

Logic Units (LUT4)	1152	4608	8640
Hard Core Processor	/	Cortex - M3	/
S-SRAM	4K bits S-SRAM	/	17280 bits S-SRAM
B-SRAM	72K bits BSRAM	180K bits B-SRAM	468K bits B-SRAM
User Flash	64K bits User Flash	256K bits User Flash	608K bits User Flash
RAM	/	64M bits HyperRAM	64M bits PSRAM
Crystal Oscillator	27Mhz	27Mhz	27Mhz
Display Interface	40P RGB screen interfaces	HDMI	HDMI, 40P RGB interfaces, 8P SPI interface
Camera	/	Optional OV2640	/
External SPI FLASH	Reserved Pads Only	32Mbit SPI Flash	32Mbit SPI FLASH
TF Card Slot	/	/	Yes
Downloader	Onboard USB - JTAG Downloader	Onboard USB - JTAG Downloader	Onboard USB - JTAG & UART Downloader

Software & Documents

Usage	FPGA	MCU	FPGA + MCU
Language	Verilog HDL / Verilog	C/C++	Verilog HDL / Verilog , C/C++
Brief Introduction	Users use hardware description language to design logic circuits	Users can download the hardware bitstream file of PicoRV to GW1NR-9 and use GW1NR-9 as a common MCU. It can run risc-v code and carry out risc-v soft core experiment	Based on PicoRV's IP core, users use Verilog to write custom hardware functions, and use C language to write the code running on PicoRV core
Applicable Person	Beginner, FPGA Developer	Risc-V Developer, Embedded Engineer	Senior Engineer

MORE REFERENCE CODES ARE CONSTANTLY UPDATED, PLEASE PAY ATTENTION TO OUR WIKI PAGE

DOCUMENTS IS FREELY AVAILABLE

```
1 localparam V_BackPorch = 35'49; //6 or 45
2 localparam V_Flase = 35'45;
3 localparam RightPixel = 35'480;
4 localparam V_FrontPorch= 35'462; //45 or #
5
6
7 localparam H_BackPorch = 35'430; //NOT: 高清晰度材料，增加边界的延迟，不
8 localparam H_Flase = 35'41;
9 localparam WidthPixel = 35'480;
10 localparam H_FrontPorch= 35'438;
11
12 localparam PixelForm = WidthPixel + H_BackPorch + H_FrontPorch;
13 localparam LineForm = RightPixel + V_BackPorch + V_FrontPorch;
```



The first is to set the parameters related to timing leading edge, trailing edge, effective pixel



Regarding the display of the leading edge and the trailing edge, as mentioned earlier, it can be combined into one existing time, that is, one can be set to 0, and the other can be set to the erasing time. Anyway, the time of the front and rear edges can be added up to meet the time requirements in the table.

```
1 always @( * or edge PixelCnt or regedge not1 ) begin
2   if ( not1 ) begin
3     LineCount <= 35'50;
4     PixelCount <= 35'50;
5   end
6   else if ( PixelCount == PixelForm ) begin
7     PixelCount <= 35'50;
8     LineCount <= (LineCount + 3'10);
9   end
10  else if ( LineCount == LineForm ) begin
11    LineCount <= 35'50;
12    PixelCount <= 35'50;
13  end
14 end
15
16 //注意高清晰度材料
17 assign LCD_HDNC = (( PixelCount == H_Flase) && ( PixelCount == (PixelForm+H_F
18 assign LCD_VDNC = ((( LineCount == V_Flase) && ( LineCount == (LineForm+V
```

This code generates a synchronization signal. It should be noted that the synchronization signal of this screen is a negative polarity enable

```
1 assign LCD_EN = ( ( PixelCount == H_BackPorch ) &&
2 ( PixelCount == PixelForm+H_FrontPorch ) &&
3 ! LineCount == H_BackPorch ) &&
```






-  Gowin_Picorv32_V1.2.1.zip
-  IPUG910-1.3E_Gowin Pico
-  IPUG913-1.3E_Gowin Pico
-  IPUG914-1.3E_Gowin Pico
-  IPUG915-1.3E_Gowin Pico
-  RN912-1.3E_Gowin PicoRV

-  SUG918-1.3E_Gowin Software Quick Start Guide.pdf
-  SUG935-1.3E_Gowin Design Physical Constraints User Guide.pdf
-  SUG937-1.01E_Gowin Software User Messages Reference.pdf
-  SUG940-1.3E_Gowin Design Timing Constraints User Guide.pdf
-  UG286-1.9.1E_Gowin Clock User Guide.pdf
-  UG289-1.9.2E_Gowin Programmable IO (GPIO) User Guide.pdf

Documentation Database

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Title	Category	Doc No.	Version	Released	Format
 Gowin I2C 2.0 SoftPOT Slave IP User Guide	User Guide	IPUG701	1.3E	30/12/2021	PDF
 Gowin DDR3 Memory Interface IP User Guide	User Guide	IPUG281	1.5E	30/12/2021	PDF
 Gowin DDR Memory Interface IP User Guide	User Guide	IPUG557	1.6E	29/11/2021	PDF
 Gowin CSIC IP User Guide	User Guide	IPUG902	1.0.1E	24/11/2021	PDF
 Gowin Flash Controller User Guide	User Guide	IPUG001	1.6E	24/11/2021	PDF

Gowin Software User Guide.pdf

Gowin FPGA Design Guide.pdf

Gowin Analyzer Oscilloscope User Guide.pdf

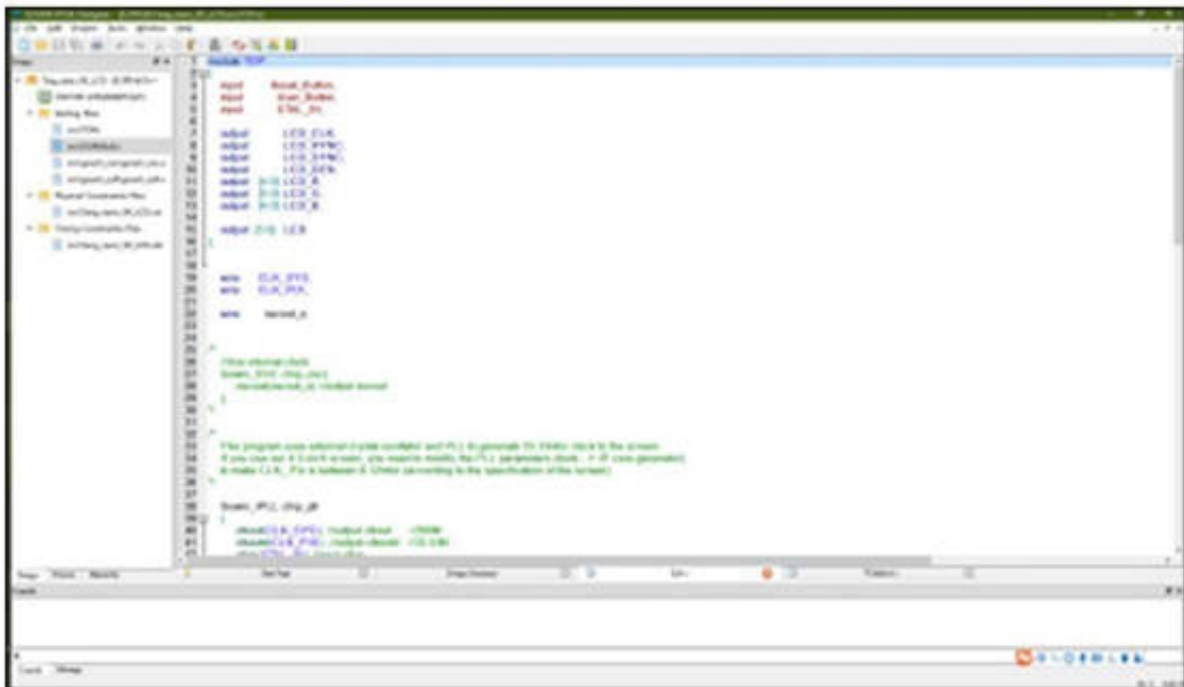
Gowin IP Core Generator User Guide.pdf

GowinSynthesis User Guide.pdf

Development Introduction

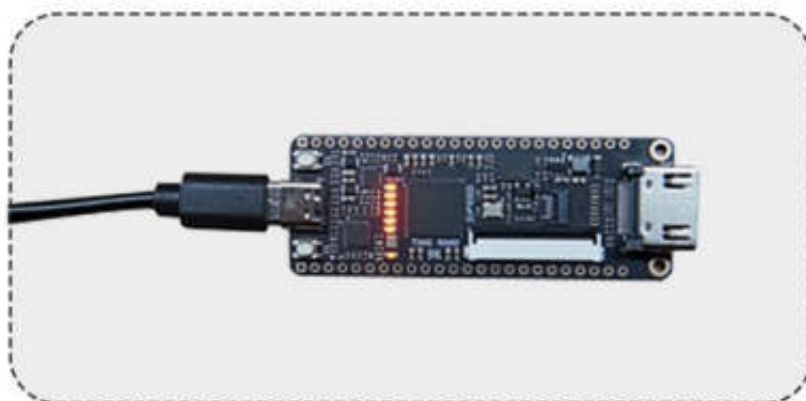
1. Development Environment

Tang nano 9K is developed using Gowin IDE, which supports general hardware description language. Gowin IDE can quickly realize IP core generation, code synthesis, layout and wiring, bitstream file generation and other related work in the process of FPGA development.



2. Download Method

Tang nano 9K is equipped with BL702 chip, which provides JTAG & UART debugging function for GW1NR-9. Users only need to use the usb-c cable to connect the development board with the computer to complete the download operation without purchasing another downloader and cumbersome wiring.



Attention

1、 It is recommended to use the following version of IDE: 1.9.6.02 (43263) to avoid failure to download.

Download link on:

Gowin official website = > Support = > GOWIN EDA home = >Download GOWIN EDA = > V1.9.6

2、 Avoid using JTAG, MODE0/1 and DONE pins. If you must use these pins, please refer to the

<UG284-1.8E_GW1N(R) Series of FPGA Products Schematic Manual.pdf>;

3、 Please pay attention to avoid static electricity hitting PCBA; Please release the static electricity from the hand before contacting PCBA;

4、 The working voltage of each GPIO has been marked in the schematic . Please do not let the actual working voltage of GPIO exceed the rated value, otherwise it will cause permanent damage to PCBA;

5、 When connecting FPC flexible cable, please ensure that the cable is completely inserted into the cable without offset;

6、 Please avoid any liquid or metal touching the pads of components on PCBA.

Community & BBS

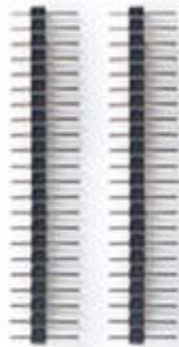
Welcome to our community.You can join us to share ideas and take technical exchanges,or get the latest information in the first time.

List

Kit



Tang Nano 9K



2.54mm Pins



Type-C Data Cable

FAQ

A. Will it be difficult for novices to start?

This development board is very suitable for novices. We recommend novices to follow the following steps to get started quickly:

1. Learn how to use IDE and drive LED according to the FPGA tutorial on our wiki page;
2. Read the massive official documents and teaching videos under the technical support page on the Gowin official website;
3. Read VHDL (hardware description language) tutorials or books and start a long way of learning;
4. When you encounter problems, you can ask other developers at TG group and BBS.

B. Why program & verify failed in SRAM mode?

Gowin FPGA sram program is default readout protected. You can't readout and verify it, unless you disable protect in IDE.

C. Why program flash failed?

Tang Nano 9K 's onboard programmer only support specified version of programmer.exe :

dl.sipeed.com/shareURL/TANG/Nano%204K/IDE

D. How to get a license?

You can download the educational version of the IDE, no need to apply for a license.

If you don't want to download the educational IDE, you can use the online license: 45.33.107.56:10559

online license server only work for GoWin V1.9.8 and lower, V1.9.6 is recommended.

E. What should I do if I encounter an error in the IDE?

See < [sug937-1.01e_Gowin Software User Messages Reference. Pdf](#) >, you can find the details and solutions of the error code in this document.

BB S:bbs.sipeed.com

Documen t:wiki.sipeed.com/hardware/en/tang/Tang-Nano-9K/Nano-9K.html

Telegrama:t.me/sipeed

E-posta: support@sipeed.com

Yüksek bulut eğitim sürümü IDE:Www.gowinsemi.com/en/support/download_eda/

(Bu bağlantı Tang nano 4K/9K eğitim IDE içindir ve bir lisans için başvurmaya gerek yoktur.)

Referans kodu:

LED sürücü/RGB LCD ekran:[Github.com/sipeed/TangNano-9K-example](https://github.com/sipeed/TangNano-9K-example)

GameBOY HDMI:[Github.com/Martoni/GbHdmi](https://github.com/Martoni/GbHdmi)

PicoRV:[Github.com/YosysHQ/picorv32](https://github.com/YosysHQ/picorv32)

Tang Nano 9K üzerinde çalışan PicoRV projesi:[Github.com/sipeed/TangNano-9K-example](https://github.com/sipeed/TangNano-9K-example)