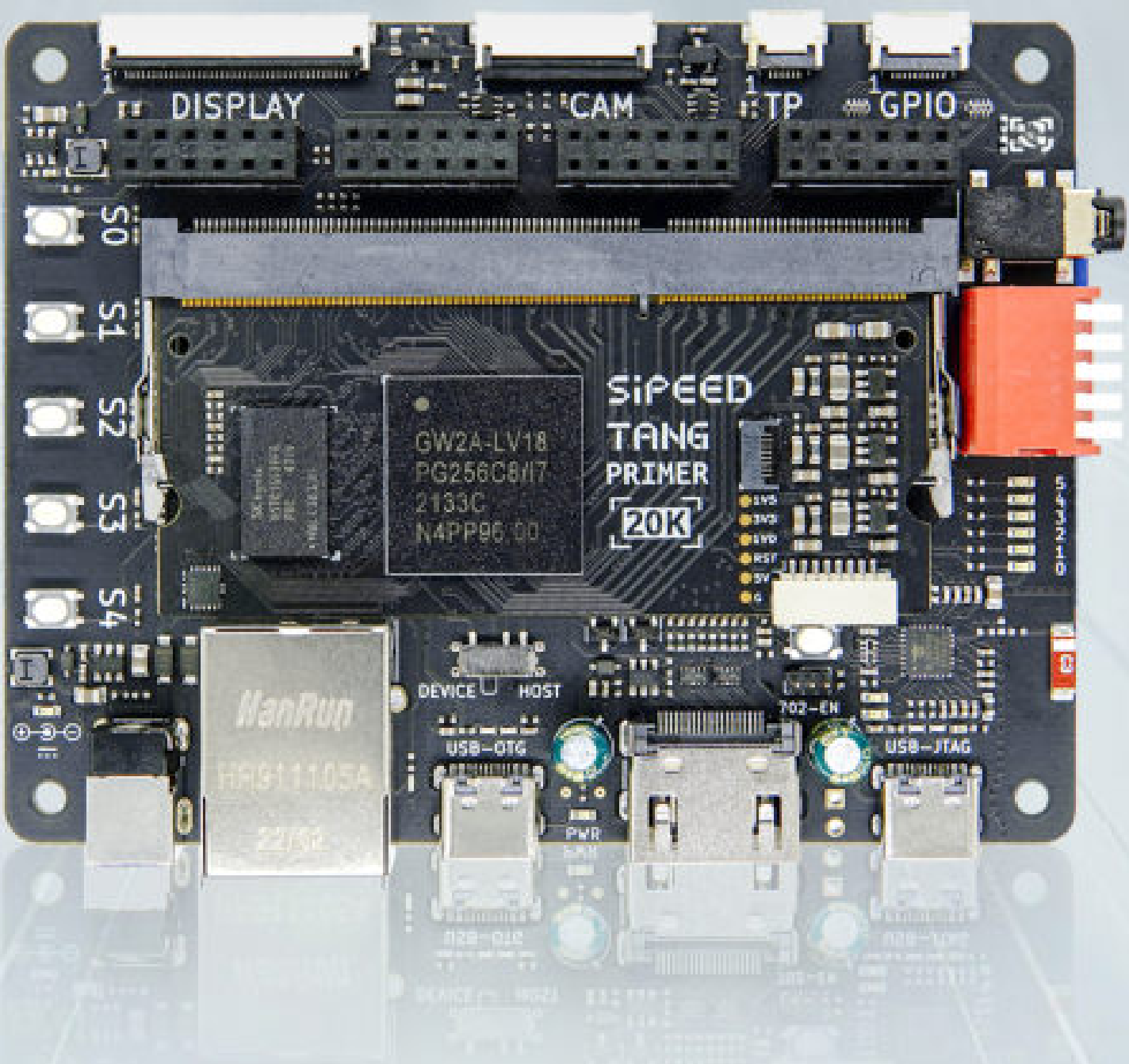
SiPEED

Tang Primer 20K

Advanced Cost-effective FPGA development board

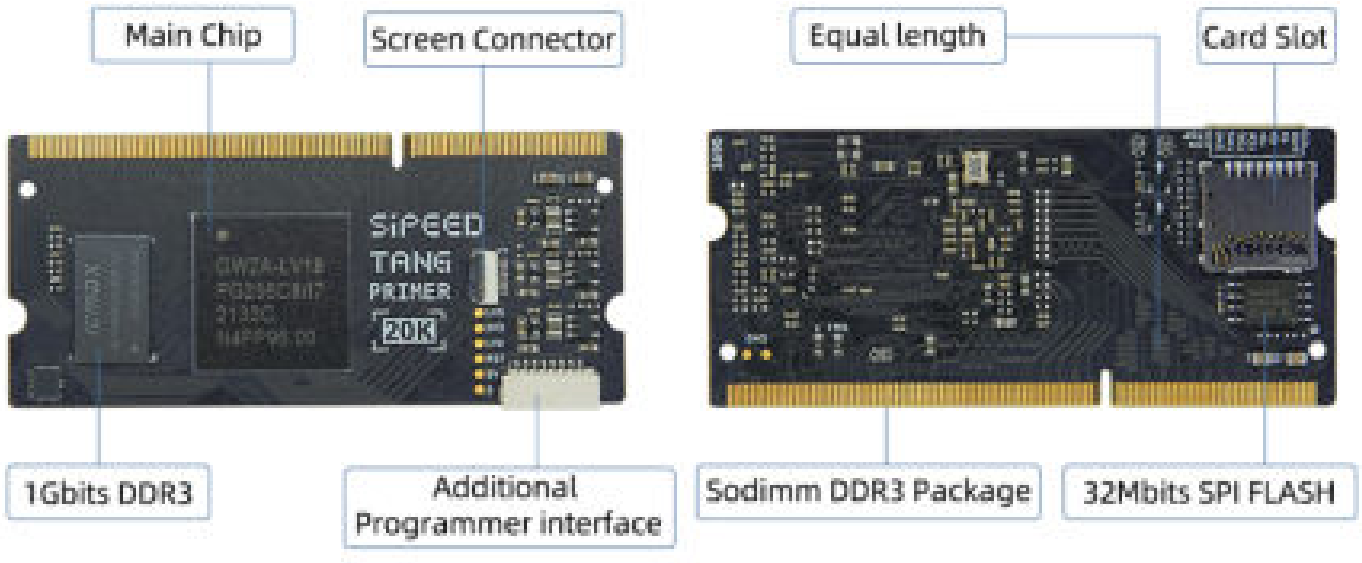


— Featurs —

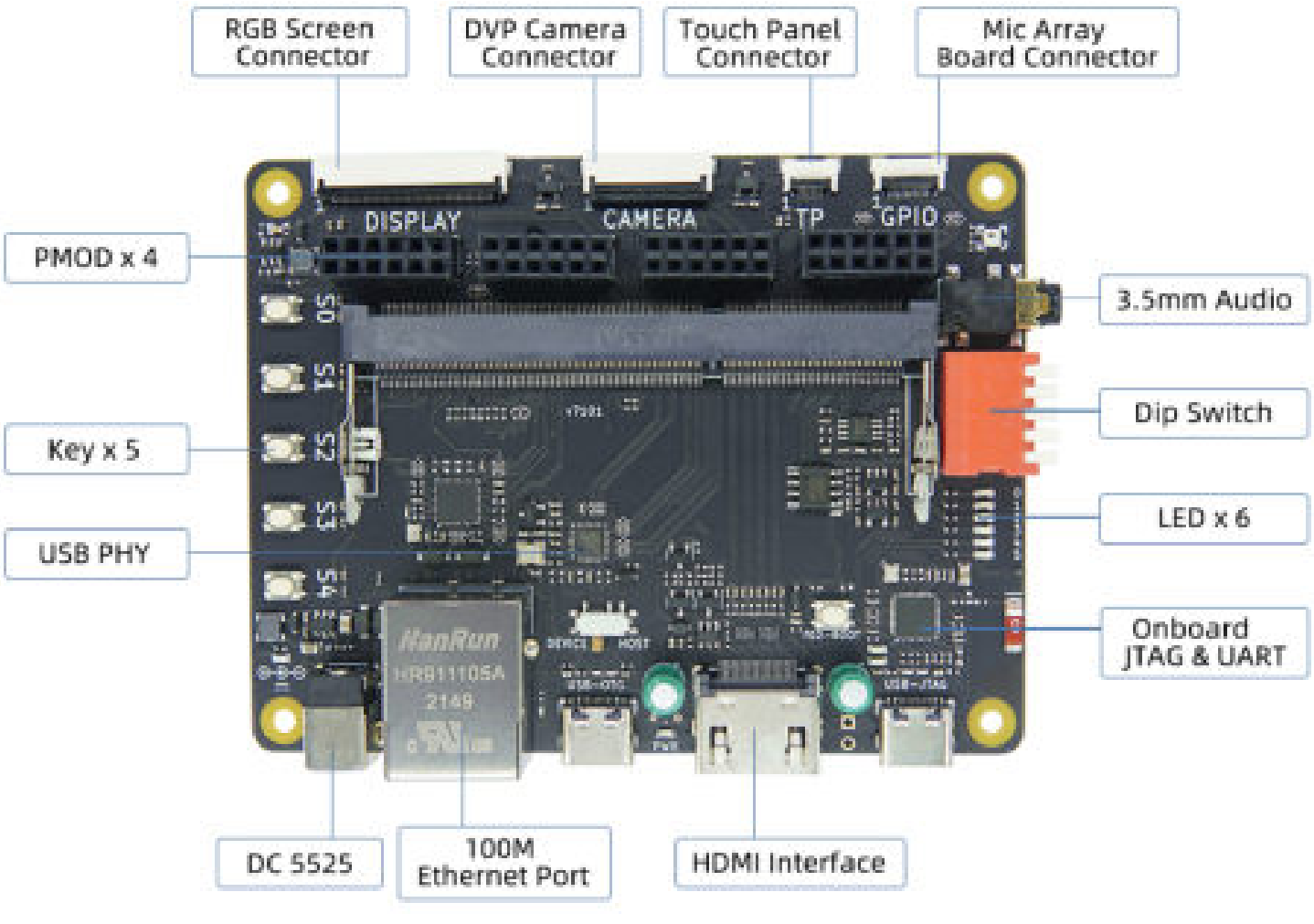
- 20K LUT4
- 1Gbit DDR3
- 10/100M ETH
- Pmod * 4
- DVP Camera
- DDR3 SODIMM
- SPI LCD
- Audio Output
- USB-UART & JTAG
- RGB LCD
- HDMI Output
- SD Card Connector
- USB2.0 PHY
- 32Mbit Flash
- MIC Array Connector

INTRODUCTION

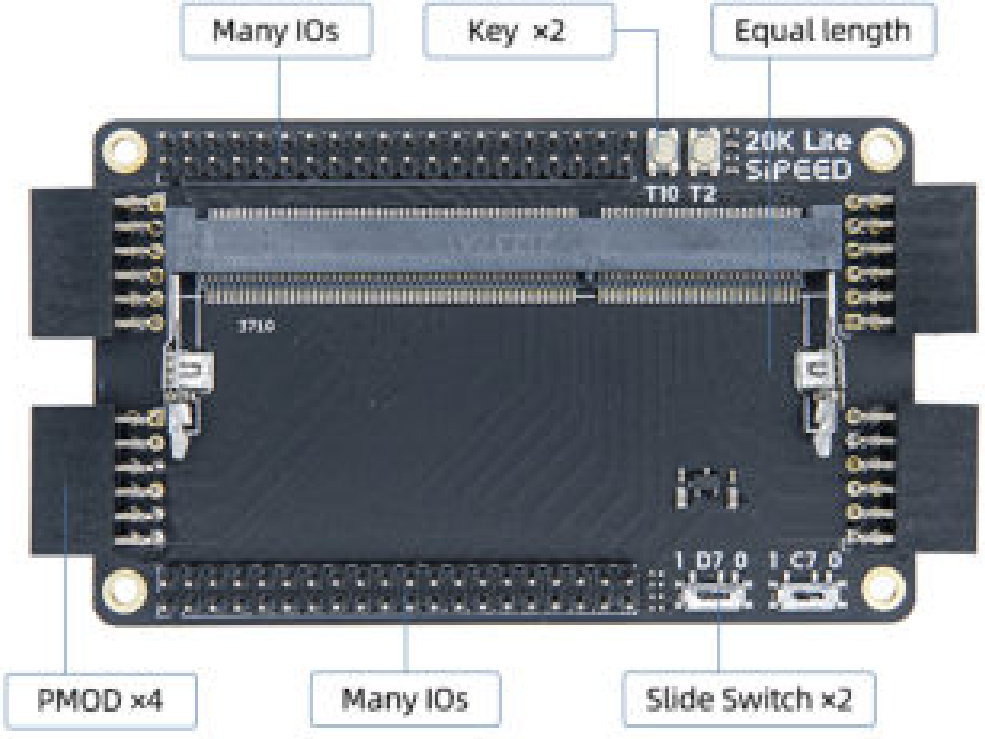
Tang Primer 20K Core Module board is sodimm package, uses GW2A-LV18PG256C8I7 as the main chip, and has multiple internal resources, such as high-performance DSP, high-speed LVDS interface and BSRAM resources, on-board DDR3 and PMIC. Users could use this CM board for rapid development and verify, and it's suitable for high-speed and low-cost situations .



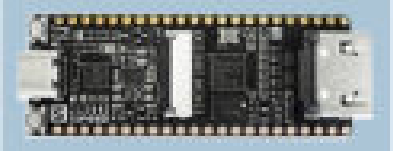
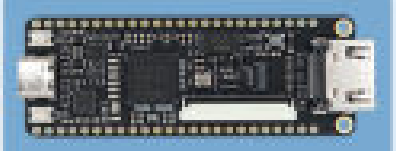
Tang Primer 20K Dock is equipped with a wealth of peripheral resources, such as onboard USB-JTAG & UART peripheral , Ethernet PHY and RJ45 connector, USB2.0 PHY, HDMI output connector, Audio output circuit and 3.5mm connector, RGB screen connector,DVP camera connector。



Tang Primer 20K Lite ext-board routes so many IOs to double row pin headers and PMOD interfaces, with which users could easily connect other peripheral modules or circuits for secondary development.



COMPARED

	Tang Primer 20K	Tang Nano 4K	Tang Nano 9K
Image			
Board model	Tang Primer 20K	Tang Nano 4K	Tang Nano 9K
Logic Units (LUT4)	20736	4608	8640
Available IO interfaces	104	32	45
Hardcore processor	×	Cortex-M3	×
S-SRAM	41472 bits	×	17280 bits
B-SRAM	828k bits	180k bits	468k bits
User Flash	×	256k bits	608k bits
RAM	1G bits DDR3	64M bits HyperRAM	64M bits PSRAM
Crystal Oscillator	27Mhz	27Mhz	27Mhz
Display Interface	8P SPI screen interface	HDMI	HDMI 40P RGB Interface 8P SPI screen interface
Camera	×	Optional OV2640	×
External SPI FLASH	32M bits SPI FLASH	32M bits SPI FLASH	32M bits SPI FLASH
TF card slot	√	×	√
Programmer	×	Onboard USB-JTAG Programmer	Onboard USB-JTAG& UART Programmer

PRODUCT USAGE

FPGA

Language: Verilog HDL/VHDL

Introduction: Users use hardware description language to design logic circuits

Target users: Beginner, FPGA Developer

MCU

Language: C/C++

Introduction: Users can burn the hardware code bitstream file of PicoRV/LiteX to GW2A, and then use GW2A as a common MCU. It can run RISC-V code, conduct RISC-V soft core experiments

Target users: RISC-V Developer, Embedded Engineer

FPGA+MCU

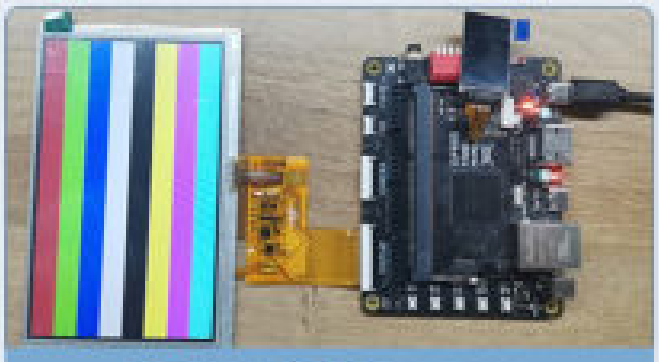
Language: Verilog HDL/VHDL , C/C++

Introduction: Users use Verilog to design custom hardware functions on the basic of PicoRV/LiteX IP core, and at the same time use C language to write code running on PicoRV/LiteX core

Target users: Senior Engineer

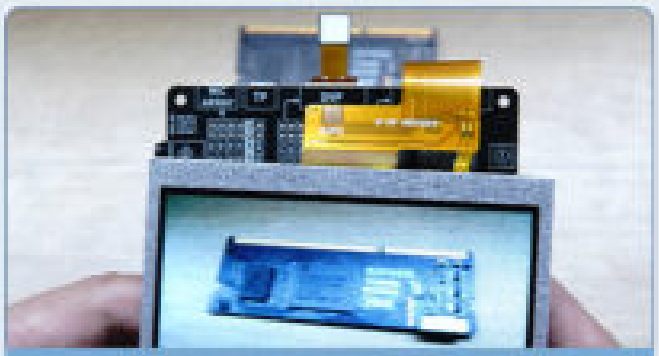
ADVANTAGES

Mutiple Usages:

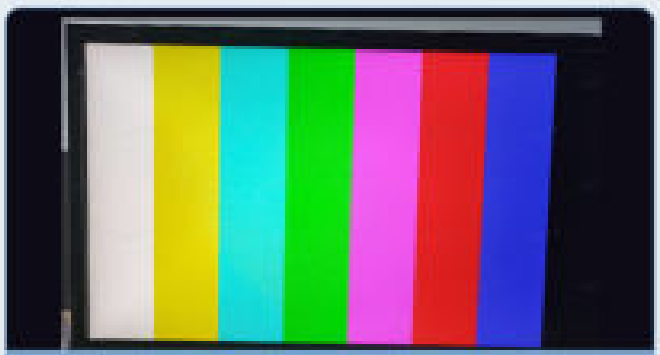


Drive RGB Screen

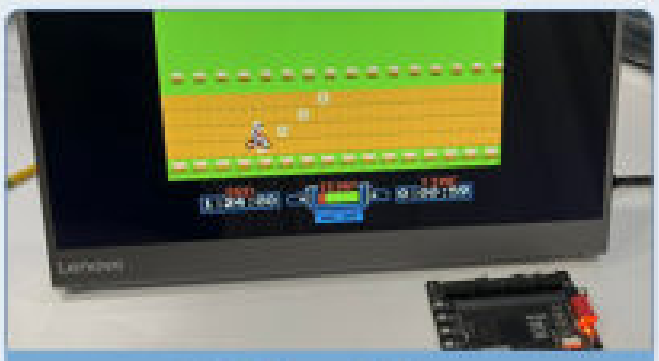
Drive SPI Screen



Display Camera Content



Drive HDMI Screen



FC Simulator

Mic Array Board test

Drive PMOD

Visit github.com/sipeed/TangPrimer-20K-example for more examples.

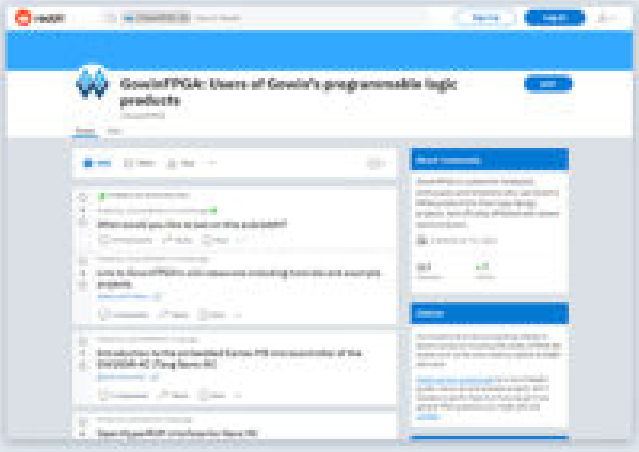
Documents and Forum:

Documents and use guide webpage

wiki.sipeed.com

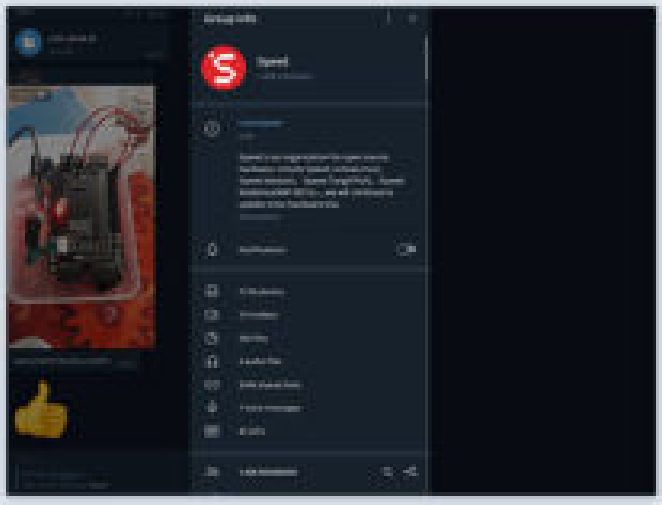
Online technical exchange forum

reddit.com/r/GowinFPGA/



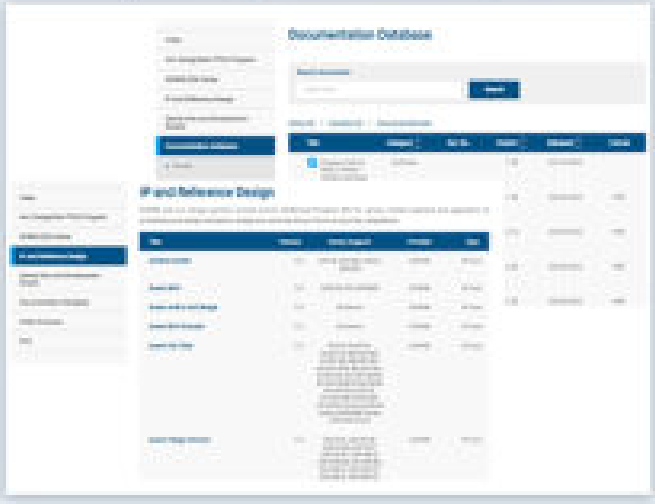
Online chat group

https://t.me/sipeed



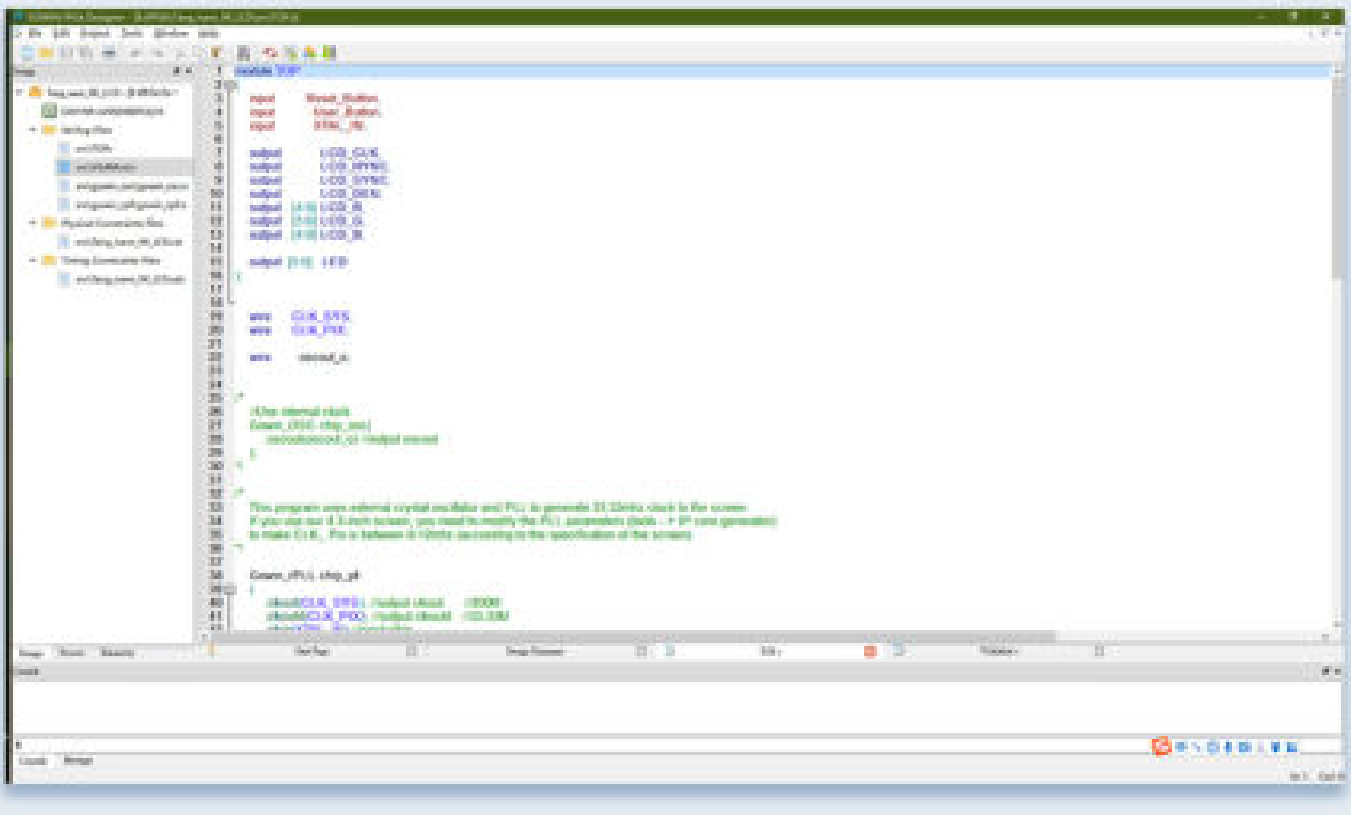
Official datasheet and IP core

https://www.gowinsemi.com/en/support/



IDE:

Comapred with other FPGA IDE, the IDE which is used to develop Tang Primer 20K is really small, the hard disk capacity occupied after installation does not exceed 1G. And this IDE is really fast, from which users will exclaim the speed of Synthesize and Plase&Route can be so fast.



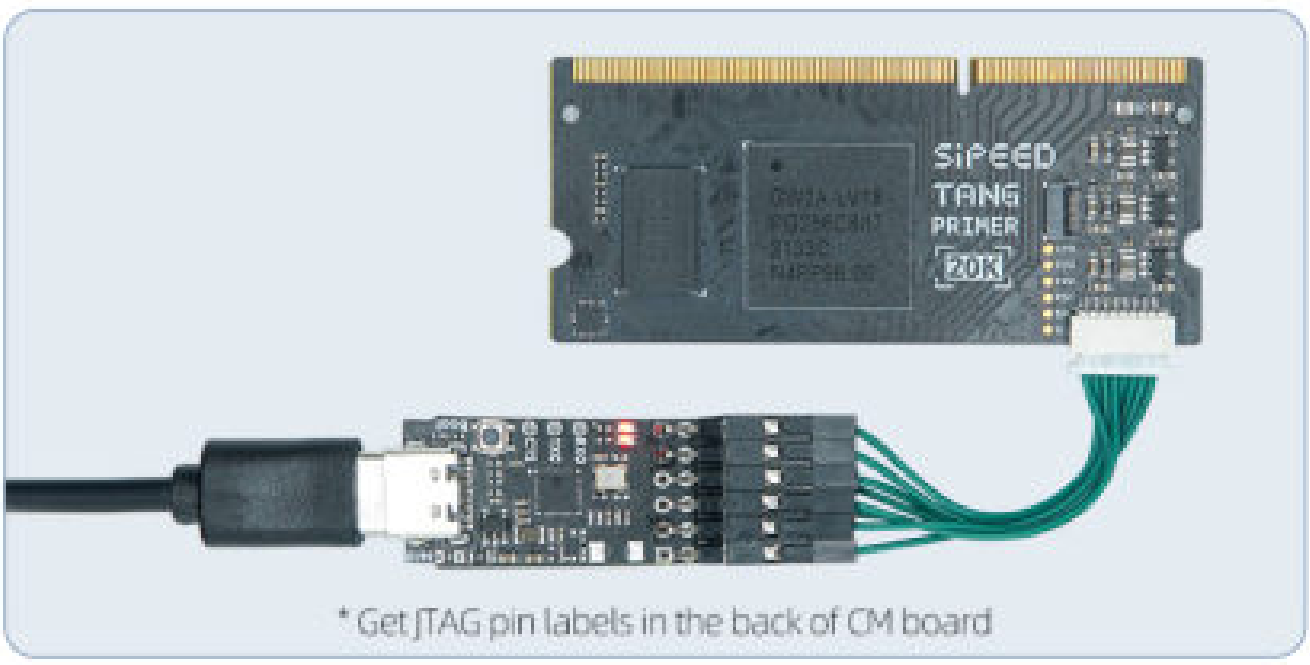
OTHERS

Burnning:

Burn without DOCK ext-board

Tang Primer 20K CM board can download biststream by RV debugger plus with connecting cable like below.

CM Board	5V0	TMS	TDO	TCK	TDI	RX	TX	GND
Debugger	5V0	TMS	TDO	TCK	TDI	TX	RX	GND



* Get JTAG pin labels in the back of CM board

Burn with DOCK ext-board

Tang Primer 20K Dock contains onboard JTAG&UART, with which to help user to burn bitstream.

Additional Notes:

Documents:	wiki.sipeed.com/en/primer20k
Examples	github.com/sipeed/TangPrimer-20K-example
LiteX :	github.com/enjoy-digital/litex
DDR Example:	github.com/ZiyangYE/LicheeTang20K_DDR_Test
Gowin IP Core:	https://www.gowinsemi.com/en/support/
Forum:	reddit.com/r/GowinFPGA/
Online Group:	https://t.me/sipeed
Business email:	support@sipeed.com

Belge: Wiki.sipeed.com/en/primer20k

Github: Github.com/sipeed/TangPrimer-20K-example

Forum: Reddit.com/r/GowinFPGA/

Telgraf:T. me/sipeed

İş e-postası: Support@sipeed.com

Resmi veri sayfası ve IP çekirdeği: Www.gowinsemi.com/en/support/

PRECAUTIONS

1、It is recommended to use the educational edition IDE, because it's license free. If you need the IP core or other features that the education edition does not provide, you can consider using the Business edition IDE, but you need to apply for a license from Gowin.

2、The device selected in IDE is GW2A-LV18PG256C8/I7, while the device selected in Programmer application is GW2A-18C.

3、Avoid using JTAG, MODE, DONE, these pins. If you must use these pins, please check: UG206-1.8_GW2A(R) Series FPGA Product Schematic Instruction Manual.pdf for more information.

4、Please pay attention to avoid static electricity hitting the PCBA; please discharge the static electricity from the hands before touching the PCBA.

5、The working voltage of each GPIO has been marked in the schematic diagram, please do not let the actual working voltage of the GPIO exceed the rated value, otherwise it will cause permanent damage to the PCBA.

6、When connecting the FPC flexible cable, please ensure that the cable is inserted into the flexible cable ompletely without any offset.

7、Please avoid any liquid and metal touching the pads of the components on the PCBA during the power-on process, otherwise it will cause a short circuit and burn the PCBA.

SHIPPING LIST

Core Broad

20K Core Broad*1

8P 1.0mm to 2.54mm
Terminal wires *1

One

RV debugger
plus *1

Type-C
Data Cabble*1

8P 1.0mm to 2.54mm
Terminal wires*1

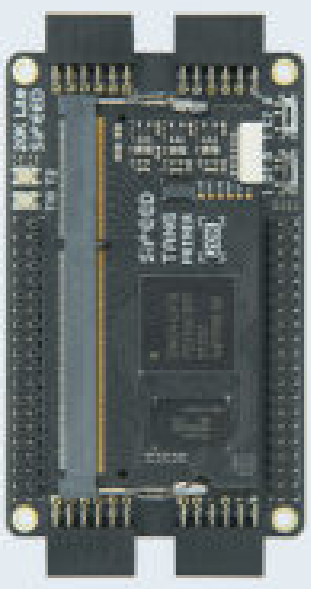
20K
Core Broad*1

Two

RV debugger
plus *1

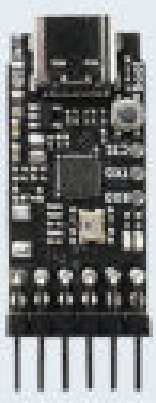
Type-C
Data Cabble*1

8P 1.0mm to 2.54mm
Terminal wires*1



20K Core Broad*1
20K Lite ext-board*1

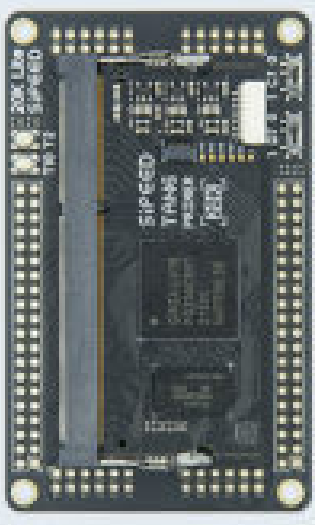
Three



RV debugger
plus *1

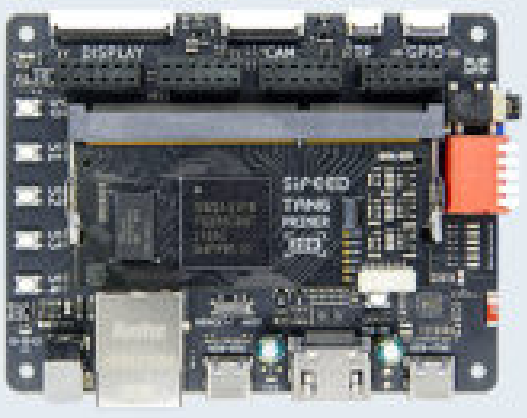
Type-C
Data Cabble*1

8P 1.0mm to 2.54mm
Terminal wires*1



20K Core Broad*1
20K Lite ext-board
(no pin header) *1

Four

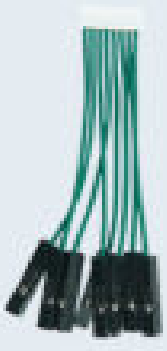


20K Core Broad*1
20K Dock ext-board*1

1.27mm black
pin header cap*2

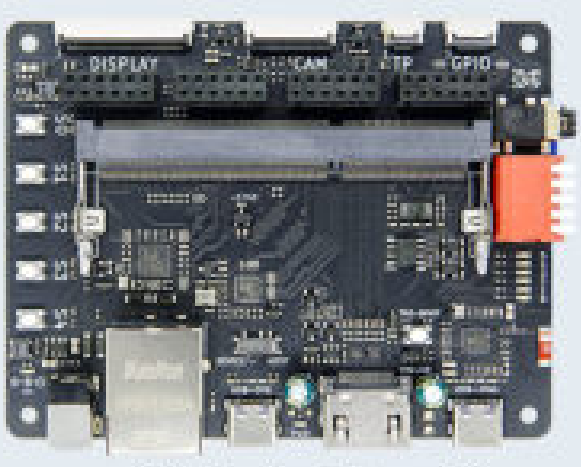
USB-C OTG
Convertor *1

Type-C
Data Cabble*1

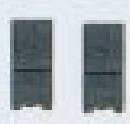


8P 1.0mm to 2.54mm
Terminal wires*1

Five



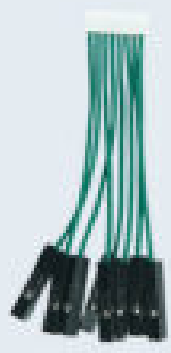
20K Dock ext-board*1



1.27mm black
pin header cap*2

USB-C OTG
Convertor*1

Type-C
Data Cabble*1



8P 1.0mm to 2.54mm
Terminal wires*1

FAQ

1、Will it be difficult for to start?

Visit wiki.sipeed.com/en/primer20k to start fpga journey

2、What if I meet trouble?

Visit our Online Documents, join our Online Group or visit Online Forum for solution.

3、How to get a license?

Apply to Gowin official to get a license.