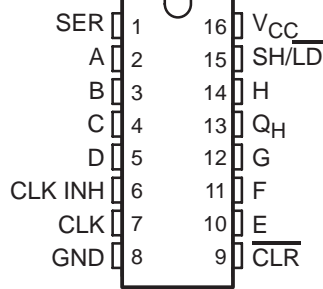


SN54HC166, SN74HC166 8-BIT PARALLEL-LOAD SHIFT REGISTERS

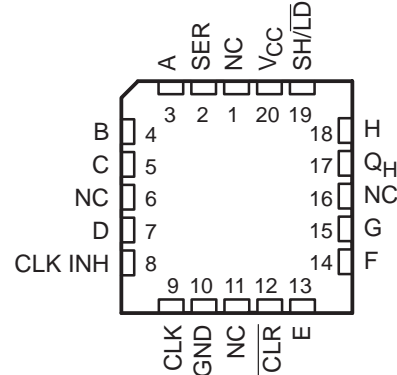
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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 13$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Synchronous Load
- Direct Overriding Clear
- Parallel-to-Serial Conversion

SN54HC166 . . . J OR W PACKAGE
SN74HC166 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC166 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

ORDERING INFORMATION

| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|--------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube of 25 | SN74HC166N | SN74HC166N |
| | SOIC – D | Tube of 40 | SN74HC166D | HC166 |
| | | Reel of 2500 | SN74HC166DR | |
| | | Reel of 250 | SN74HC166DT | |
| | SOP – NS | Reel of 2000 | SN74HC166NSR | HC166 |
| | SSOP – DB | Reel of 2000 | SN74HC166DBR | HC166 |
| -55°C to 125°C | TSSOP – PW | Tube of 90 | SN74HC166PW | HC166 |
| | | Reel of 2000 | SN74HC166PWR | |
| | | Reel of 250 | SN74HC166PWT | |
| -55°C to 125°C | CDIP – J | Tube of 25 | SNJ54HC166J | SNJ54HC166J |
| | CFP – W | Tube of 150 | SNJ54HC166W | SNJ54HC166W |
| | LCCC – FK | Tube of 55 | SNJ54HC166FK | SNJ54HC166FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HC166, SN74HC166

8-BIT PARALLEL-LOAD SHIFT REGISTERS

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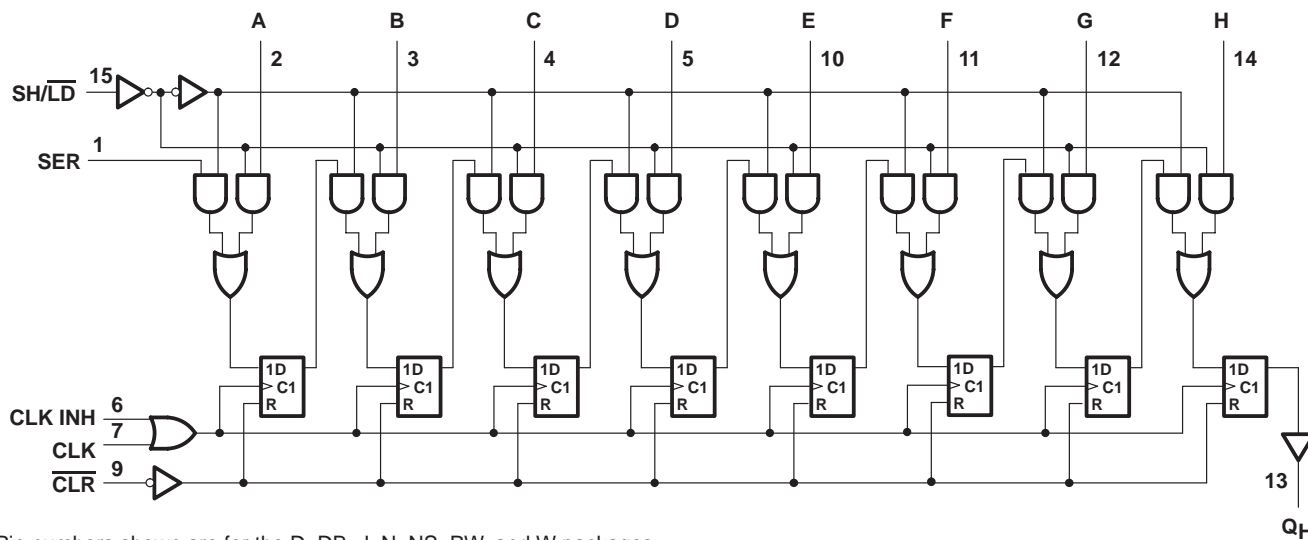
description/ordering information (continued)

These parallel-in or serial-in, serial-out registers feature gated clock (CLK, CLK INH) inputs and an overriding clear ($\overline{\text{CLR}}$) input. The parallel-in or serial-in modes are established by the shift/load ($\text{SH}/\overline{\text{LD}}$) input. When high, $\text{SH}/\overline{\text{LD}}$ enables the serial (SER) data input and couples the eight flip-flops for serial shifting with each clock (CLK) pulse. When low, the parallel (broadside) data inputs are enabled, and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of CLK through a 2-input positive-NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either CLK or CLK INH high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. $\overline{\text{CLR}}$ overrides all other inputs, including CLK, and resets all flip-flops to zero.

FUNCTION TABLE

| INPUTS | | | | | | OUTPUTS | | |
|-------------------------|----------------------------------|---------|------------|-----|-----------------------|----------|----------|----------|
| | | | | | | INTERNAL | | Q_H |
| $\overline{\text{CLR}}$ | $\text{SH}/\overline{\text{LD}}$ | CLK INH | CLK | SER | PARALLEL A . . . H | Q_A | Q_B | |
| L | X | X | X | X | X | L | L | L |
| H | X | L | L | X | X | Q_{A0} | Q_{B0} | Q_{H0} |
| H | L | L | \uparrow | X | a . . . h | a | b | h |
| H | H | L | \uparrow | H | X | H | Q_{An} | Q_{Gn} |
| H | H | L | \uparrow | L | X | L | Q_{An} | Q_{Gn} |
| H | X | H | \uparrow | X | X | Q_{A0} | Q_{B0} | Q_{H0} |

logic diagram (positive logic)

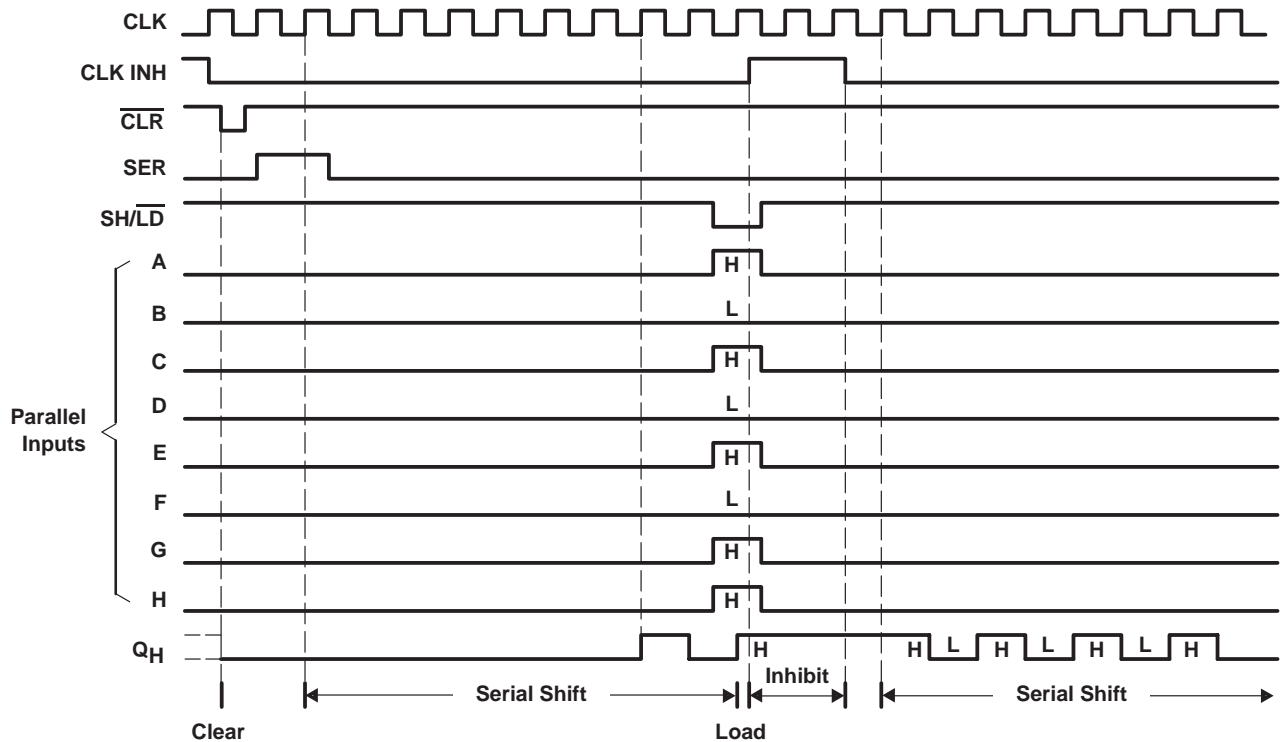


Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

SN54HC166, SN74HC166 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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typical clear, shift, load, inhibit, and shift sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ± 20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 25 mA |
| Continuous current through V_{CC} or GND | ± 50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 73°C/W |
| DB package | 82°C/W |
| N package | 67°C/W |
| NS package | 64°C/W |
| PW package | 108°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC166, SN74HC166

8-BIT PARALLEL-LOAD SHIFT REGISTERS

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recommended operating conditions (see Note 3)

| | | SN54HC166 | | | SN74HC166 | | | UNIT |
|-----------------------------|---------------------------------|-------------------------|----------|------|-----------|----------|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2\text{ V}$ | | 1.5 | 1.5 | | V | |
| | | $V_{CC} = 4.5\text{ V}$ | | 3.15 | 3.15 | | | |
| | | $V_{CC} = 6\text{ V}$ | | 4.2 | 4.2 | | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2\text{ V}$ | | 0.5 | | 0.5 | V | |
| | | $V_{CC} = 4.5\text{ V}$ | | 1.35 | | 1.35 | | |
| | | $V_{CC} = 6\text{ V}$ | | 1.8 | | 1.8 | | |
| V_I | Input voltage | 0 | V_{CC} | | 0 | V_{CC} | | V |
| V_O | Output voltage | 0 | V_{CC} | | 0 | V_{CC} | | V |
| $\Delta t/\Delta v^\dagger$ | Input transition rise/fall time | $V_{CC} = 2\text{ V}$ | | 1000 | | 1000 | | ns |
| | | $V_{CC} = 4.5\text{ V}$ | | 500 | | 500 | | |
| | | $V_{CC} = 6\text{ V}$ | | 400 | | 400 | | |
| T_A | Operating free-air temperature | -55 | 125 | | -40 | 85 | | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

† If this device is used in the threshold region (from $V_{IL\text{max}} = 0.5\text{ V}$ to $V_{IH\text{min}} = 1.5\text{ V}$), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_f = 1000\text{ ns}$ and $V_{CC} = 2\text{ V}$ does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC166 | | SN74HC166 | | UNIT | |
|-----------|--------------------------------|-----------------------------|------------|--------------------------|-----------|-----------|-----------|------------|-----------|------------|------|---------------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | | |
| V_{OH} | $V_I = V_{IH}$ or V_{IL} | $I_{OH} = -20\ \mu\text{A}$ | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V | | |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | | |
| | | $I_{OH} = -4\text{ mA}$ | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | | |
| | | | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | | |
| V_{OL} | $V_I = V_{IH}$ or V_{IL} | $I_{OL} = 20\ \mu\text{A}$ | 2 V | | 0.002 | 0.1 | | 0.1 | | V | | |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | | | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | | | |
| | | $I_{OL} = 4\text{ mA}$ | 4.5 V | | 0.17 | 0.26 | | 0.4 | | | 0.33 | |
| | | | 6 V | | 0.15 | 0.26 | | 0.4 | | | 0.33 | |
| I_I | $V_I = V_{CC}$ or 0 | | 6 V | | ± 0.1 | ± 100 | | ± 1000 | | ± 1000 | nA | |
| I_{CC} | $V_I = V_{CC}$ or 0, $I_O = 0$ | | 6 V | | | | 8 | | 160 | | 80 | μA |
| C_i | | | 2 V to 6 V | | 3 | 10 | | 10 | | | 10 | pF |



SN54HC166, SN74HC166 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HC166 | | SN74HC166 | | UNIT | | |
|-------------------------|--|--|-----------------------|-----|-----------|-----|-----------|-----|------|--|----|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | | | |
| f _{clock} | Clock frequency | 2 V | 6 | | 4.2 | | 5 | | MHz | | |
| | | 4.5 V | 31 | | 21 | | 25 | | | | |
| | | 6 V | 36 | | 25 | | 29 | | | | |
| t _w | $\overline{\text{CLR}}$ low | 2 V | 100 | | 150 | | 125 | | ns | | |
| | | 4.5 V | 20 | | 30 | | 25 | | | | |
| | | 6 V | 17 | | 26 | | 21 | | | | |
| | CLK high or low | 2 V | 80 | | 120 | | 100 | | | | |
| | | 4.5 V | 16 | | 24 | | 20 | | | | |
| | | 6 V | 14 | | 20 | | 17 | | | | |
| t _{su} | SH/ $\overline{\text{LD}}$ high before CLK↑ | 2 V | 145 | | 220 | | 180 | | ns | | |
| | | 4.5 V | 29 | | 44 | | 36 | | | | |
| | | 6 V | 25 | | 38 | | 31 | | | | |
| | SER before CLK↑ | 2 V | 80 | | 120 | | 100 | | | | |
| | | 4.5 V | 16 | | 24 | | 20 | | | | |
| | | 6 V | 14 | | 20 | | 17 | | | | |
| | CLK INH low before CLK↑ | 2 V | 100 | | 150 | | 125 | | | | |
| | | 4.5 V | 20 | | 30 | | 25 | | | | |
| | | 6 V | 17 | | 26 | | 21 | | | | |
| | Data before CLK↑ | 2 V | 80 | | 120 | | 100 | | | | |
| | | 4.5 V | 16 | | 24 | | 20 | | | | |
| | | 6 V | 14 | | 20 | | 17 | | | | |
| | $\overline{\text{CLR}}$ inactive before CLK↑ | 2 V | 40 | | 60 | | 50 | | | | |
| | | 4.5 V | 8 | | 12 | | 10 | | | | |
| | | 6 V | 7 | | 10 | | 9 | | | | |
| | t _h | SH/ $\overline{\text{LD}}$ high after CLK↑ | 2 V | 0 | | 0 | | 0 | | | ns |
| | | | 4.5 V | 0 | | 0 | | 0 | | | |
| | | | 6 V | 0 | | 0 | | 0 | | | |
| SER after CLK↑ | | 2 V | 5 | | 5 | | 5 | | | | |
| | | 4.5 V | 5 | | 5 | | 5 | | | | |
| | | 6 V | 5 | | 5 | | 5 | | | | |
| CLK INH high after CLK↑ | | 2 V | 0 | | 0 | | 0 | | | | |
| | | 4.5 V | 0 | | 0 | | 0 | | | | |
| | | 6 V | 0 | | 0 | | 0 | | | | |
| Data after CLK↑ | | 2 V | 5 | | 5 | | 5 | | | | |
| | | 4.5 V | 5 | | 5 | | 5 | | | | |
| | | 6 V | 5 | | 5 | | 5 | | | | |



SN54HC166, SN74HC166

8-BIT PARALLEL-LOAD SHIFT REGISTERS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

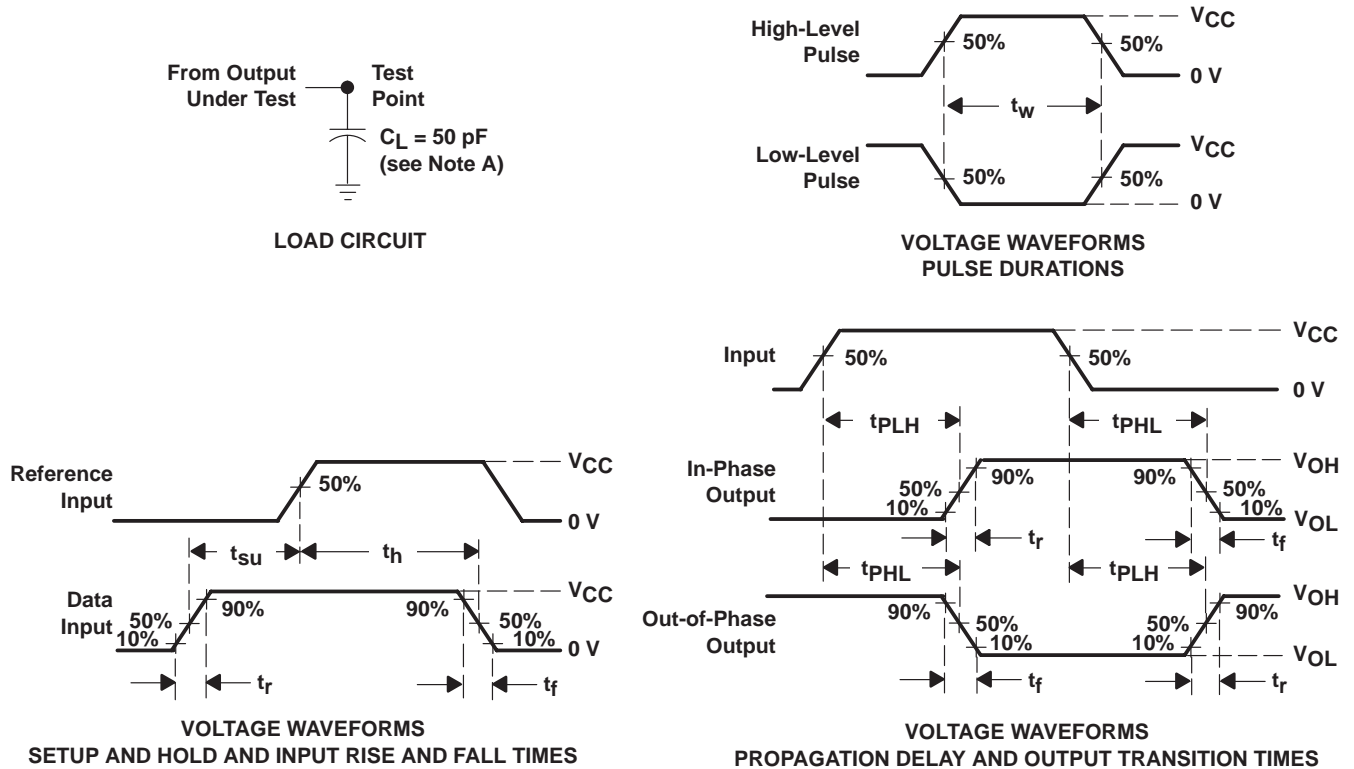
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC166 | | SN74HC166 | | UNIT |
|-----------|------------------|-------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 2 V | 6 | 11 | | 4.2 | | 5 | MHz | |
| | | | 4.5 V | 31 | 36 | | 21 | | 25 | | |
| | | | 6 V | 36 | 45 | | 25 | | 29 | | |
| t_{PHL} | \overline{CLR} | Q_H | 2 V | | 62 | 120 | | 180 | | 150 | ns |
| | | | 4.5 V | | 18 | 24 | | 36 | | 30 | |
| | | | 6 V | | 13 | 20 | | 31 | | 26 | |
| t_{pd} | CLK | Q_H | 2 V | | 75 | 150 | | 225 | | 190 | ns |
| | | | 4.5 V | | 15 | 30 | | 45 | | 38 | |
| | | | 6 V | | 13 | 26 | | 38 | | 32 | |
| t_t | | Any | 2 V | | 38 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C_{pd} Power dissipation capacitance | No load | 50 | pF |



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-9050101Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-9050101QEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| 5962-9050101VEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| SN54HC166J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| SN74HC166D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166DBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166DBRE4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166DBRG4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166DT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166DTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166DTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74HC166NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74HC166NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166PWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166PWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166PWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| | | | | | | no Sb/Br) | | |
| SN74HC166PWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166PWTE4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC166PWTE4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SNJ54HC166FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54HC166J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

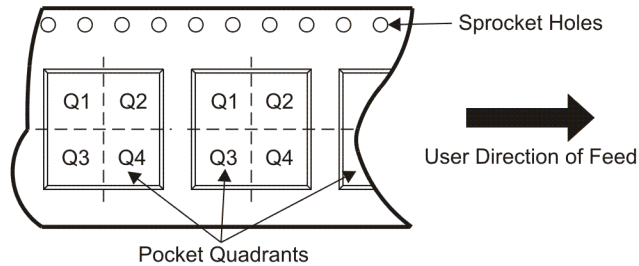
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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC166DBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC166DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC166NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC166PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC166DBR | SSOP | DB | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74HC166DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HC166NSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74HC166PWR | TSSOP | PW | 16 | 2000 | 346.0 | 346.0 | 29.0 |

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

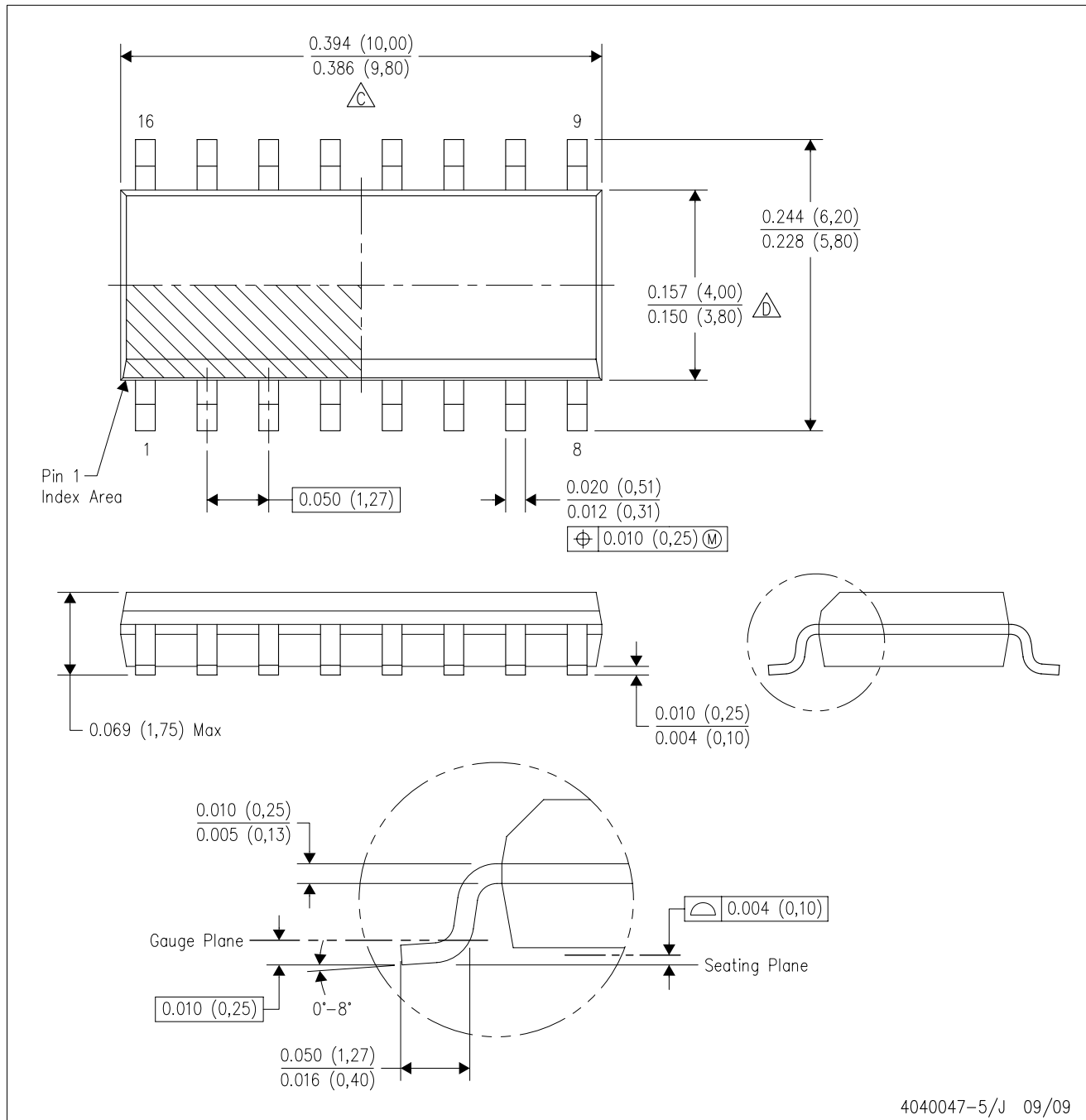
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

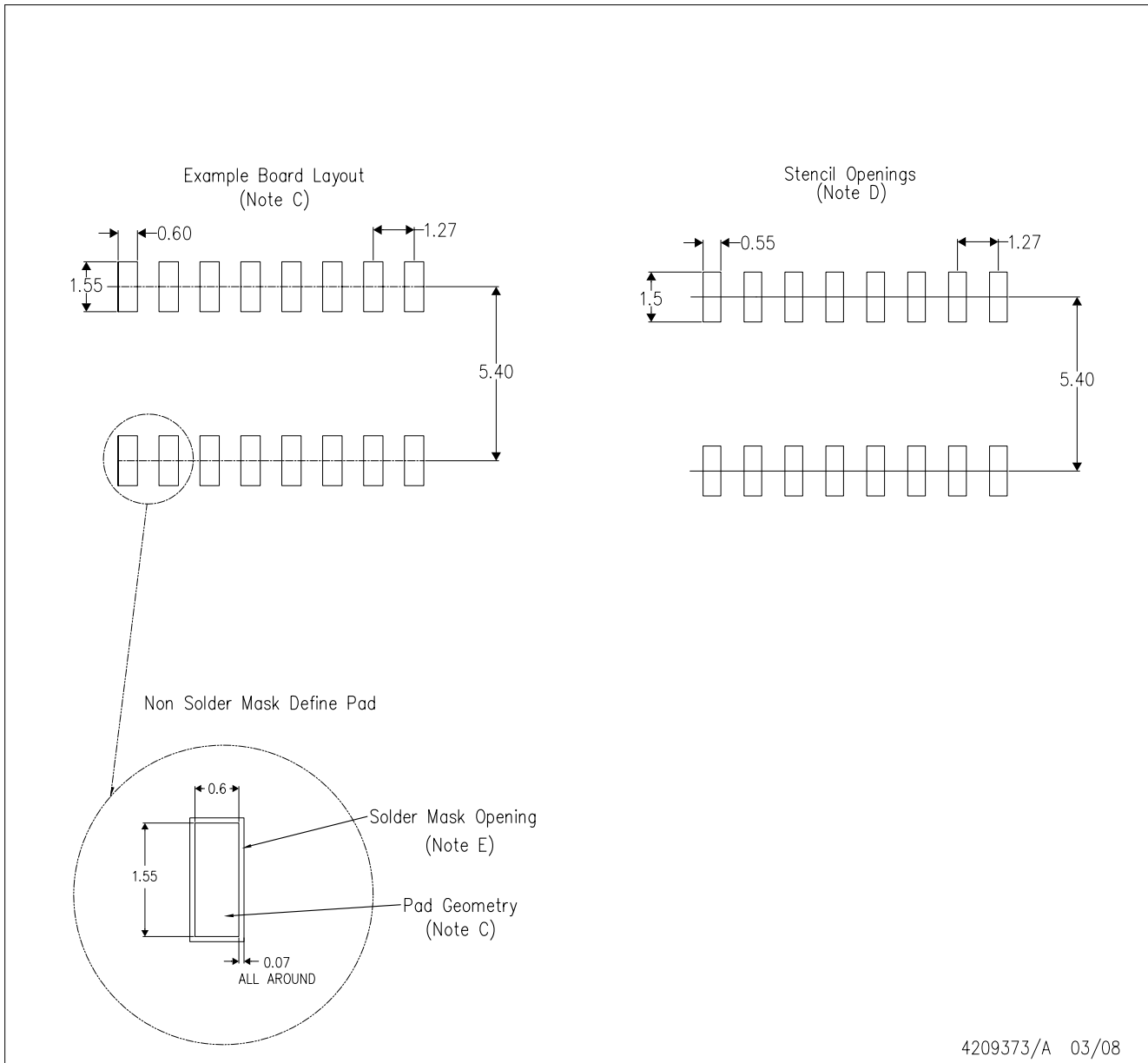
D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---|-------------------------|
| 5962-9050101Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 9050101Q2A SNJ54HC 166FK | Samples |
| 5962-9050101QEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9050101QE A SNJ54HC166J | Samples |
| 5962-9050101VEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9050101VE A SNV54HC166J | Samples |
| SN54HC166J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54HC166J | Samples |
| SN74HC166D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC166 | Samples |
| SN74HC166DBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC166 | Samples |
| SN74HC166DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 85 | HC166 | Samples |
| SN74HC166DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC166 | Samples |
| SN74HC166DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC166 | Samples |
| SN74HC166N | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC166N | Samples |
| SN74HC166NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC166 | Samples |
| SN74HC166PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC166 | Samples |
| SN74HC166PWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC166 | Samples |
| SN74HC166PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 85 | HC166 | Samples |
| SN74HC166PWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC166 | Samples |
| SNJ54HC166FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|-------------------------|----------------------|--------------|------------------------------------|----------------|
| | | | | | | | | | | 9050101Q2A SNJ54HC 166FK | |
| SNJ54HC166J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9050101QE A SNJ54HC166J | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HC166, SN54HC166-SP, SN74HC166 :

- Catalog: [SN74HC166](#), [SN54HC166](#)
- Military: [SN54HC166](#)
- Space: [SN54HC166-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC166DBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC166DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC166DR | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC166DRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC166PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC166PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC166PWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC166DBR | SSOP | DB | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74HC166DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HC166DR | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74HC166DRG4 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HC166PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74HC166PWR | TSSOP | PW | 16 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74HC166PWT | TSSOP | PW | 16 | 250 | 367.0 | 367.0 | 35.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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