

PNP Power Transistor

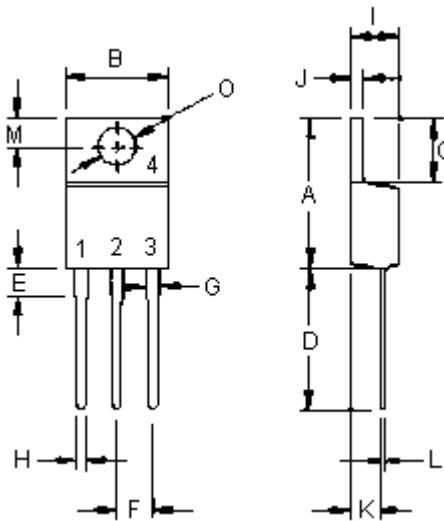


Complementary Silicon Plastic Power Transistors

Features:

Designed for use in general purpose power amplifier and switching applications.

- Collector-emitter sustaining voltage- $V_{CEO(sus)} = 100V$ (minimum).
- Collector-emitter saturation voltage- $V_{CE(sat)} = 1.5V$ (maximum) at $I_C = 6.0A$.
- Current gain-bandwidth product $f_T = 3.0$ MHz (minimum) at $I_C = 500mA$.



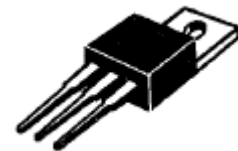
- Pin 1. Base.
 2. Collector.
 3. Emitter.
 4. Collector (Case).

Dimensions	Minimum	Maximum
A	14.68	15.31
B	9.78	10.42
C	5.01	6.52
D	13.06	14.62
E	3.57	4.07
F	2.42	3.66
G	1.12	1.36
H	0.72	0.96
I	4.22	4.98
J	1.14	1.38
K	2.20	2.97
L	0.33	0.55
M	2.48	2.98
O	3.70	3.90

Dimensions : Millimetres

PNP
TIP42C

6 Ampere
 Complementary Silicon
 Power Transistors
 40 to 100 Volts
 65 Watts



TO-220

Maximum Ratings

Characteristic	Symbol	TIP42C	Unit
Collector-Emitter Voltage	V_{CEO}	100	V
Collector-Base Voltage	V_{CBO}		
Emitter-Base Voltage	V_{EBO}		
Collector Current - Continuous - Peak	I_C	6 10	A
Base Current	I_B	2	
Total Power Dissipation at $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	65 0.52	W W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-65 to +150	$^\circ C$

<http://www.farnell.com>
<http://www.newark.com>
<http://www.cpc.co.uk>



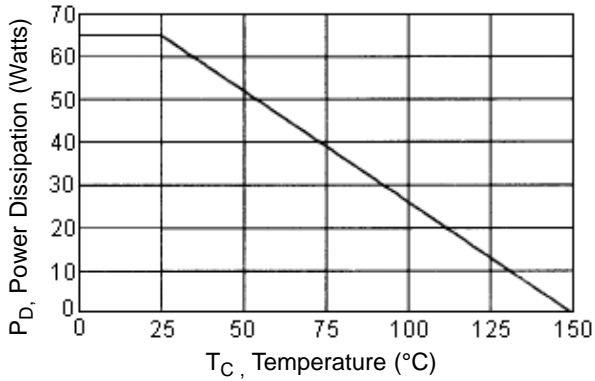
PNP Power Transistor



Thermal Characteristics

Characteristic	Symbol	Maximum	Unit
Thermal Resistance Junction to Case	$R_{\theta jc}$	1.92	$^{\circ}\text{C}/\text{W}$

Power Derating



Electric Characteristics ($T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristics	Symbol	Minimum	Maximum	Units
Off Characteristics				
Collector-Emitter Sustaining Voltage (1) ($I_C = 30\text{mA}$, $I_B = 0$)	$V_{CEO(sus)}$	100	-	V
Collector Cut-off Current ($V_{CE} = 60\text{V}$, $I_B = 0$)	I_{CEO}	-	0.7	mA
Collector Cut-off Current ($V_{CE} = 100\text{V}$, $V_{EB} = 0$)	I_{CES}	-	0.4	
Emitter Cut-off Current ($V_{EB} = 5.0\text{V}$, $I_C = 0$)	I_{EBO}	-	1.0	
On Characteristics (1)				
DC Current Gain ($I_C = 0.3\text{A}$, $V_{CE} = 4.0\text{V}$) ($I_C = 0.3\text{A}$, $V_{CE} = 4.0\text{V}$)	h_{FE}	30 15	75	-
Collector-Emitter Saturation Voltage ($I_C = 6.0\text{A}$, $I_B = 600\text{mA}$)	$V_{CE(sat)}$	-	1.5	V
Base-Emitter on Voltage ($I_C = 6.0\text{A}$, $V_{CE} = 4.0\text{V}$)	$V_{BE(on)}$	-	2.0	
Dynamic Characteristics				
Current Gain-Bandwidth Product (2) ($I_C = 500\text{mA}$, $V_{CE} = 10\text{V}$, $f_{TEST} = 1\text{MHz}$)	f_T	3.0	-	MHz
Small Signal Current Gain ($I_C = 500\text{mA}$, $V_{CE} = 10\text{V}$, $f = 1\text{kHz}$)	h_{fe}	20	-	-

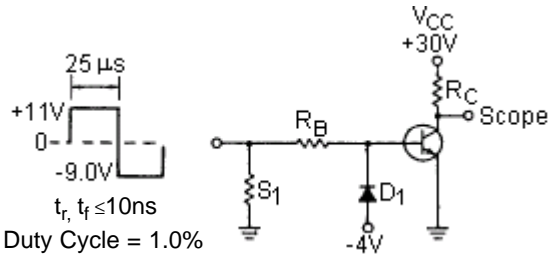
(1) Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

(2) $f_T = |h_{fe}| \cdot f_{TEST}$

PNP Power Transistor



Switching Time Test Circuit



$t_r, t_f \leq 10\text{ns}$
Duty Cycle = 1.0%

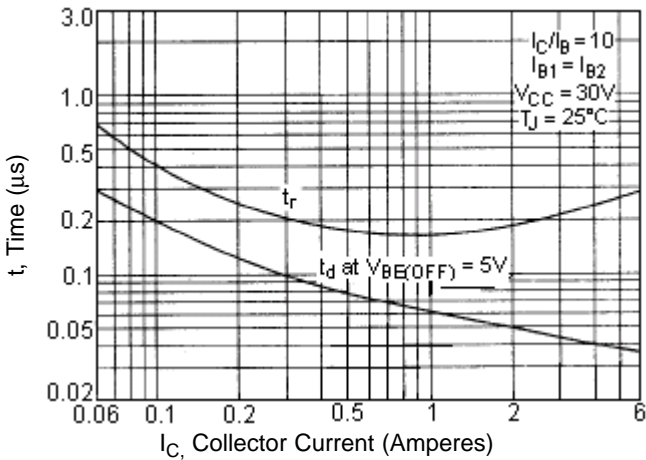
R_B and R_C Varied to Obtain Desired Current Levels

D1 Must be Fast Recovery Type. eg:

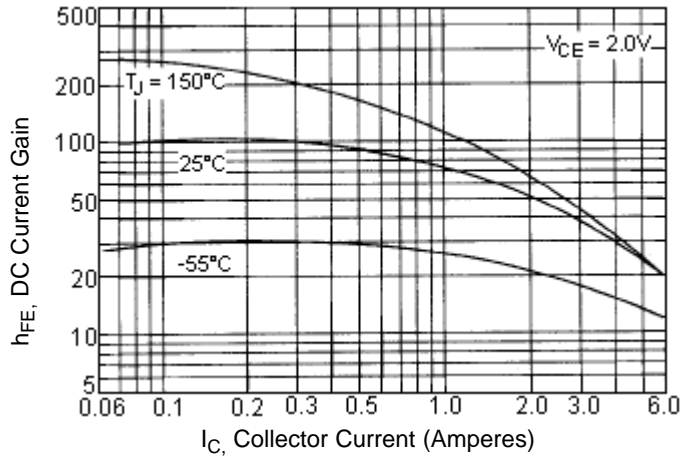
MBD5000 used Above $I_B = 100\text{mA}$

MSD6100 used Below $I_S = 100\text{mA}$

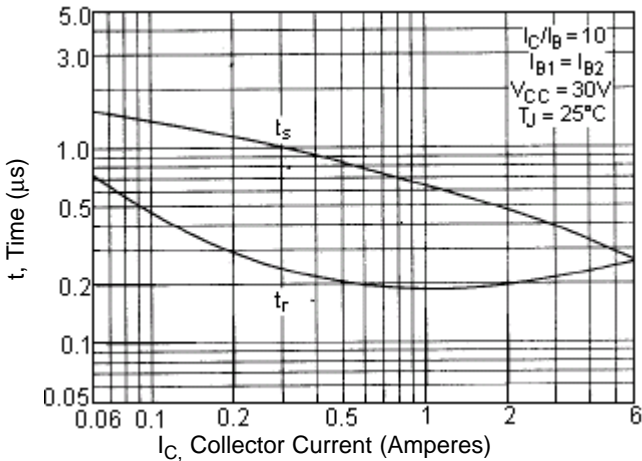
Turn-on Time



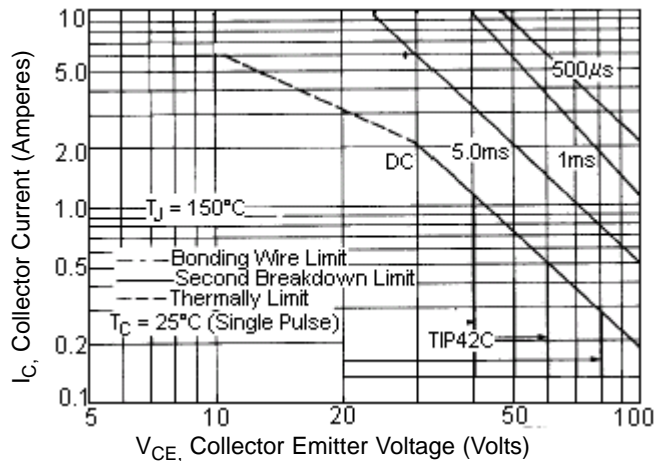
DC Current Gain



Turn-off Time



Active Region Safe Operating Area



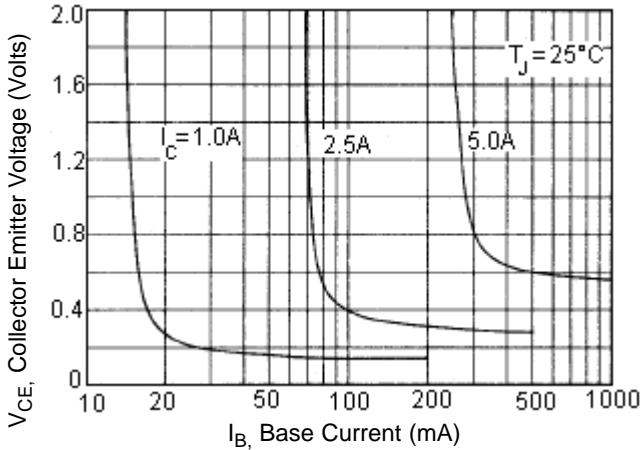
PNP Power Transistor



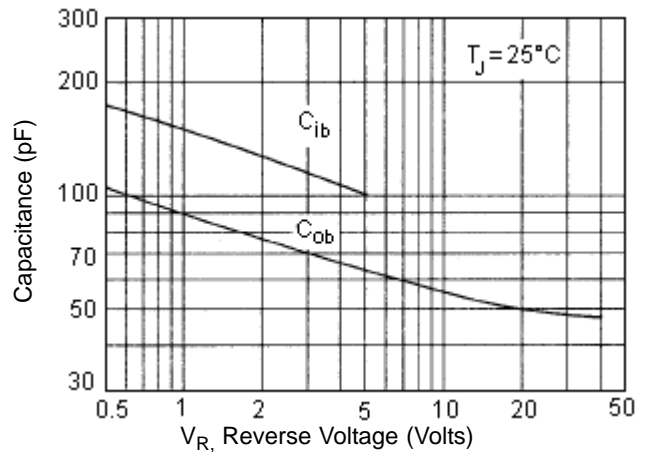
There are two limitation on the power handling ability of a transistor: average junction temperature and second breakdown safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e. the transistor must not be subjected to greater dissipation than curves indicate.

The data of curve is base on $T_{J(PK)} = 150^\circ\text{C}$; T_C is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(PK)} \leq 150^\circ\text{C}$, At high case temperatures, thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

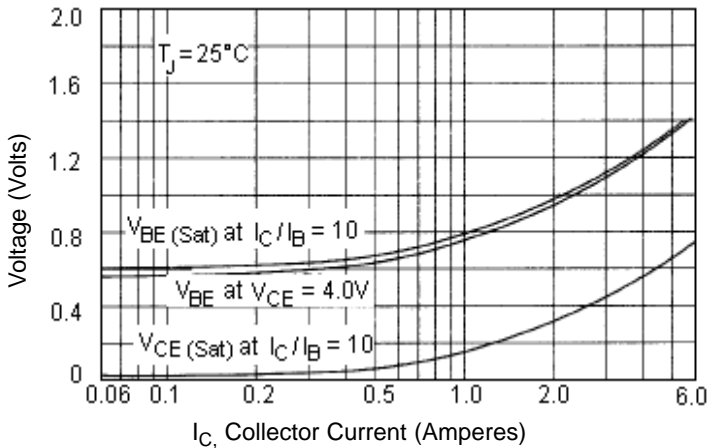
Collector Saturation Region



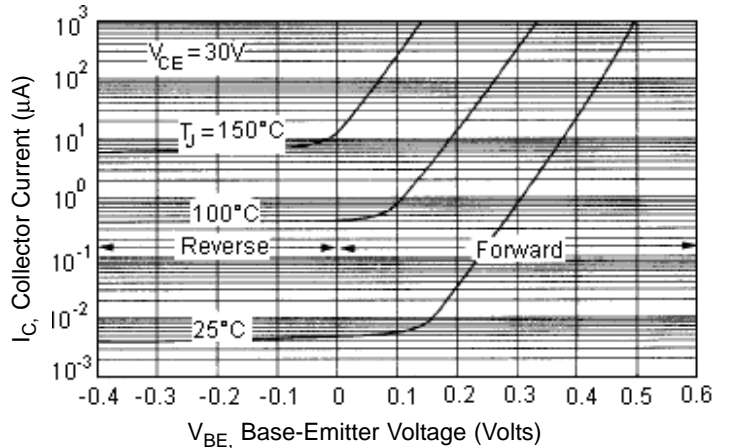
Capacitances



"ON" Voltage



Collector Cut-off Region



Part Number Table

Description	Part Number
PNP Power Transistor	TIP42C

Disclaimer This data sheet and its contents (the "Information") belong to the Premier Farnell Group (the "Group") or are licensed to it. No licence is granted for the use of it other than for information purposes in connection with the products to which it relates. No licence of any intellectual property rights is granted. The Information is subject to change without notice and replaces all data sheets previously supplied. The Information supplied is believed to be accurate but the Group assumes no responsibility for its accuracy or completeness, any error in or omission from it or for any use made of it. Users of this data sheet should check for themselves the Information and the suitability of the products for their purpose and not make any assumptions based on information included or omitted. Liability for loss or damage resulting from any reliance on the Information or use of it (including liability resulting from negligence or where the Group was aware of the possibility of such loss or damage arising) is excluded. This will not operate to limit or restrict the Group's liability for death or personal injury resulting from its negligence. MULTICOMP is the registered trademark of the Group. © Premier Farnell plc 2011.