TPS54360 60-V Input, 3.5-A, Step-Down DC/DC Converter With Eco-Mode™

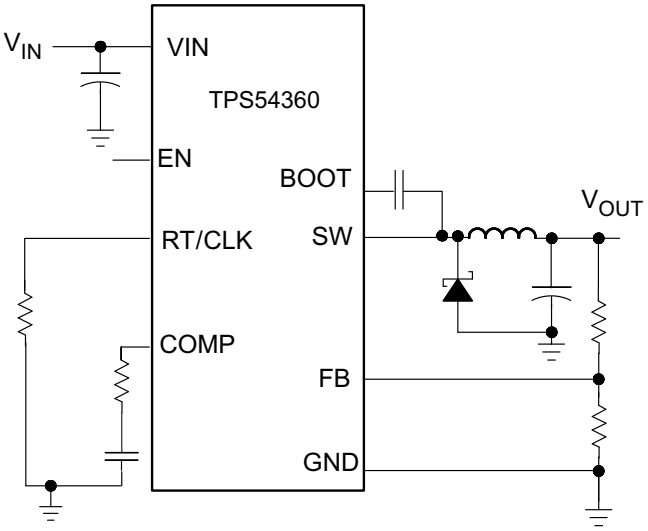
1 Features

- 4.5-V to 60-V (65-V Abs Max) Input Range
- 3.5-A Continuous Current, 4.5-A Minimum Peak Inductor Current Limit
- Current Mode Control DC/DC Converter
- 92-mΩ High-Side MOSFET
- High Efficiency at Light Loads with Pulse Skipping Eco-mode™
- Low Dropout at Light Loads with Integrated BOOT Recharge FET
- 146-μA Operating Quiescent Current
- 2-μA Shutdown Current
- 100-kHz to 2.5-MHz Fixed Switching Frequency
- Synchronizes to External Clock
- Adjustable UVLO Voltage and Hysteresis
- Internal Soft Start
- Accurate Cycle-by-Cycle Current Limit
- Thermal, Overvoltage, and Frequency Foldback Protection
- 0.8 V 1% Internal Voltage Reference
- 8-Terminal HSOIC with PowerPAD™ Package
- –40°C to 150°C T_J Operating Range
- Create a Custom Design using the TPS54360 with the WEBENCH® Power Designer

2 Applications

12-V, 24-V and 48-V Industrial, Automotive and Communications Power Systems

Simplified Schematic



3 Description

The TPS54360 is a 60-V, 3.5-A, step-down regulator with an integrated high side MOSFET. The device survives load dump pulses up to 65 V per ISO 7637. Current mode control provides simple external compensation and flexible component selection. A low ripple pulse skip mode reduces the no load supply current to 146 μA. Shutdown supply current is reduced to 2 μA when the enable pin is pulled low.

Undervoltage lockout is internally set at 4.3 V but can be increased using the enable pin. The output voltage start-up ramp is internally controlled to provide a controlled start-up and eliminate overshoot.

A wide switching frequency range allows either efficiency or external component size to be optimized. Frequency foldback and thermal shutdown protect internal and external components during an overload condition.

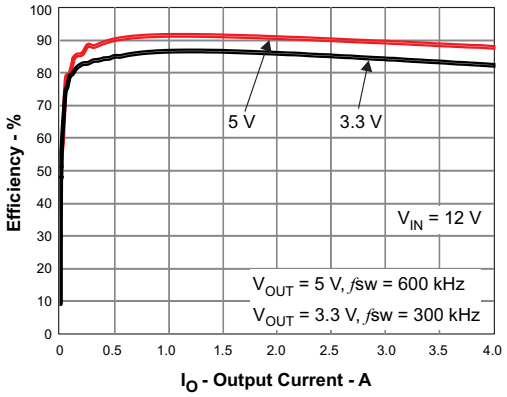
The TPS54360 is available in an 8-terminal thermally enhanced HSOIC PowerPAD™ package.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
TPS54360	HSOIC (8)	4.89 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency vs Load Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2017) to Revision G — **Page**

- Added top navigator icon for TI reference design ... 1
- Added VBOOT clamping stipulation to Equation 2 ... 15

Changes from Revision E (March 2014) to Revision F — **Page**

- Added the WEBENCH information in the *Features*, *Detailed Design Procedure*, and *Device Support* sections ... 1
- Changed the *Handling Ratings* table to the *ESD Ratings* table ... 5
- Moved the Storage temperature to the *Absolute Maximum Ratings* table ... 5
- Changed V_{IN} MIN Value From: 4.5 V To: $V_O + V_{DO}$, and added Note 1 in the *Recommended Operating Conditions* ... 5
- Updated text and added Equation 1 and Equation 2 in *Low Dropout Operation and Bootstrap Voltage (BOOT)* ... 14
- Deleted text: "The start and stop voltage for a typical 5 V..." and Figure: "5V Start/Stop Voltage" from the *Low Dropout Operation and Bootstrap Voltage (BOOT)* section ... 14
- Changed Equation 7 and Equation 8 ... 16
- Changed Equation 27 ... 26
- Added new section: *Minimum V_{IN}* ... 31
- Deleted 2 graphs named "Low Dropout Operation" from the *Application Curves* section ... 34

Changes from Revision D (February 2013) to Revision E — **Page**

- Changed the data sheet to the new TI layout and added the Device Information table ... 1
- Added the *Handling Ratings* table and *Recommended Operating Conditions* table ... 5
- Changed the Operating: nonswitching supply current TEST CONDITIONS From: FB = 0.83 V To: FB = 0.9 V ... 7
- Changed RT/CLK high threshold MAX value From: 1.7 V To: 2 V ... 7
- Changed Figure 6 title From: HIGH FREQUENCY RANGE To: LOW FREQUENCY RANGE ... 8
- Changed Figure 7 title From: LOW FREQUENCY RANGE To: HIGH FREQUENCY RANGE ... 8

Changes from Revision C (October 2012) to Revision D **Page**

- Changed Figure 11 and Figure 12 From: I_{EN} (µV) To: I_{EN} (µA) 9

Changes from Revision B (September 2012) to Revision C **Page**

- Changed From: 20 mV/div To: 200 mV/div in Figure 42 34

Changes from Revision A (September 2012) to Revision B **Page**

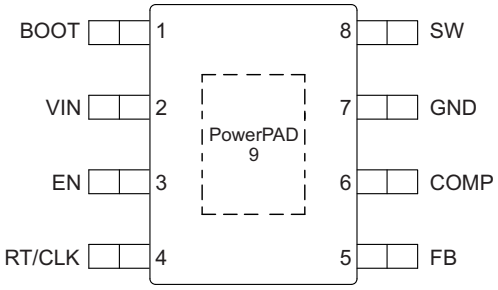
- Changed Feature From: 1 µA Shutdown Current To: 2 µA Shutdown Current 1

Changes from Original (August 2012) to Revision A **Page**

- Changed the device status From: Product Preview To: Production Data 1

5 Pin Configuration and Functions

DDA Package
8-Pin HSOIC
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and SW. If the voltage on this capacitor is below the minimum required to operate the high side MOSFET, the output is switched off until the capacitor is refreshed.
VIN	2	I	Input supply voltage with 4.5 V to 60 V operating range.
EN	3	I	Enable terminal, with internal pull-up current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors. See the *Enable and Adjusting Undervoltage Lockout* section.
RT/CLK	4	I	Resistor Timing and External Clock. An internal amplifier holds this terminal at a fixed voltage when using an external resistor to ground to set the switching frequency. If the terminal is pulled above the PLL upper threshold, a mode change occurs and the terminal becomes a synchronization input. The internal amplifier is disabled and the terminal is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to resistor frequency programming.
FB	5	I	Inverting input of the transconductance (gm) error amplifier.
COMP	6	O	Error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this terminal.
GND	7	–	Ground
SW	8	I	The source of the internal high-side power MOSFET and switching node of the converter.
Thermal Pad	9	–	GND terminal must be electrically connected to the exposed pad on the printed circuit board for proper operation.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	65	V
	EN	–0.3	8.4	
	BOOT		73	
	FB	–0.3	3	
	COMP	–0.3	3	
	RT/CLK	–0.3	3.6	
Output voltage	BOOT-SW		8	V
	SW	–0.6	65	
	SW, 10-ns transient	–2	65	
Operating junction temperature		–40	150	°C
Storage temperature, T_{STG}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		MAX	UNIT
V_{ESD} (1)	Human Body Model (HBM) ESD Stress Voltage (2)	±2000	V
	Charged Device Model (HBM) ESD Stress Voltage (3)	±500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. terminals listed as 1000 V may actually have higher performance.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. terminals listed as 250 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply input voltage(1)	$V_O + V_{DO}$	60	V
V_O	Output voltage	0.8	58.8	V
I_O	Output current	0	3.5	A
T_J	Junction temperature	–40	150	°C

(1) See Equation 1

6.4 Thermal Information

THERMAL METRIC(1)(2)		TPS54360 DDA (HSOIC) 8 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance (standard board)	42.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.4	°C/W
θ_{JCtop}	Junction-to-case(top) thermal resistance	45.8	°C/W
θ_{JCbot}	Junction-to-case(bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. See power dissipation estimate in application section of this data sheet for more information.

Thermal Information (continued)

THERMAL METRIC[1][2]		TPS54360 DDA (HSOIC) 8 PINS	UNIT
θ_{JB}	Junction-to-board thermal resistance	23.4	°C/W

6.5 Electrical Characteristics

T_J = –40°C to 150°C, V_{IN} = 4.5 to 60V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN TERMINALS)						
	Operating input voltage		4.5		60	V
	Internal undervoltage lockout threshold	Rising	4.1	4.3	4.48	V
	Internal undervoltage lockout threshold hysteresis			325		mV
	Shutdown supply current	EN = 0 V, 25°C, 4.5 V ≤ VIN ≤ 60 V		2.25	4.5	µA
	Operating: nonswitching supply current	FB = 0.9 V, T_A = 25°C		146	175	
ENABLE AND UVLO (EN TERMINALS)						
	Enable threshold voltage	No voltage hysteresis, rising and falling	1.1	1.2	1.3	V
	Input current	Enable threshold +50 mV		–4.6		µA
		Enable threshold –50 mV	–0.58	–1.2	-1.8	
	Hysteresis current		–2.2	–3.4	-4.5	µA
VOLTAGE REFERENCE						
	Voltage reference		0.792	0.8	0.808	V
HIGH-SIDE MOSFET						
	On-resistance	V_{IN} = 12 V, BOOT-SW = 6 V		92	190	mΩ
ERROR AMPLIFIER						
	Input current			50		nA
	Error amplifier transconductance (g_M)	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		350		µMhos
	Error amplifier transconductance (g_M) during soft-start	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V, V_{FB} = 0.4 V		77		µMhos
	Error amplifier dc gain	V_{FB} = 0.8 V		10,000		V/V
	Min unity gain bandwidth			2500		kHz
	Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100 mV overdrive		±30		µA
	COMP to SW current transconductance			12		A/V
CURRENT LIMIT						
	Current limit threshold	All VIN and temperatures, Open Loop(1)	4.5	5.5	6.8	A
		All temperatures, VIN = 12 V, Open Loop(1)	4.5	5.5	6.25	
		VIN = 12 V, T_A = 25°C, Open Loop(1)	5.2	5.5	5.85	
	Current limit threshold delay			60		ns
THERMAL SHUTDOWN						
	Thermal shutdown			176		°C
	Thermal shutdown hysteresis			12		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK TERMINALS)						
	Switching frequency range using RT mode		100		2500	kHz
f_{SW}	Switching frequency	R_T = 200 kΩ	450	500	550	kHz
	Switching frequency range using CLK mode		160		2300	kHz
	RT/CLK high threshold			1.55	2	V
	RT/CLK low threshold		0.5	1.2		V

(1) Open Loop current limit measured directly at the SW terminal and is independent of the inductor value and slope compensation.

6.6 Timing Requirements

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL SOFT-START TIME					
Soft-start time	f_{SW} = 500 kHz, 10% to 90%		2.1		ms
Soft-start time	f_{SW} = 2.5 MHz, 10% to 90%		0.42		ms
HIGH-SIDE MOSFET					
Minimum controllable on time	V_{IN} = 12 V, T_A = 25°C		135		ns
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK TERMINALS)					
Minimum CLK input pulse width			15		ns
RT/CLK falling edge to SW rising edge delay	Measured at 500 kHz with RT resistor in series		55		ns
PLL lock in time	Measured at 500 kHz		78		µs

6.7 Typical Characteristics

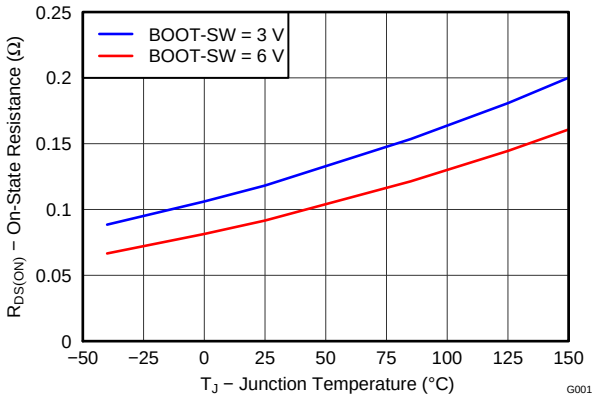


Figure 1. On Resistance vs Junction Temperature

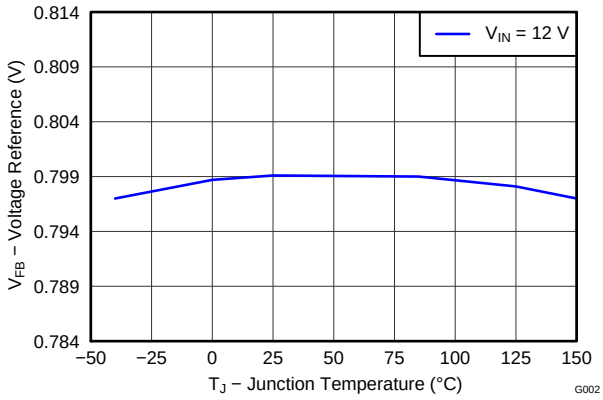


Figure 2. Voltage Reference vs Junction Temperature

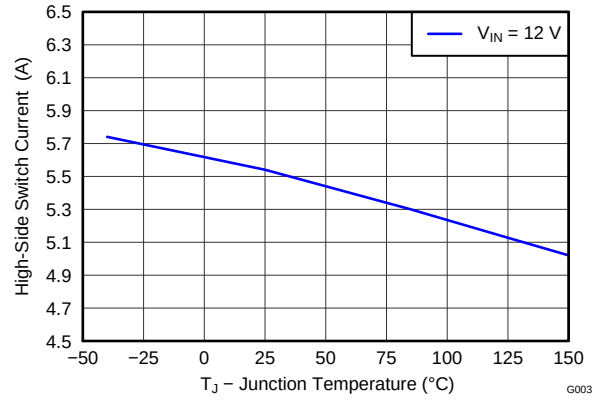


Figure 3. Switch Current Limit vs Junction Temperature

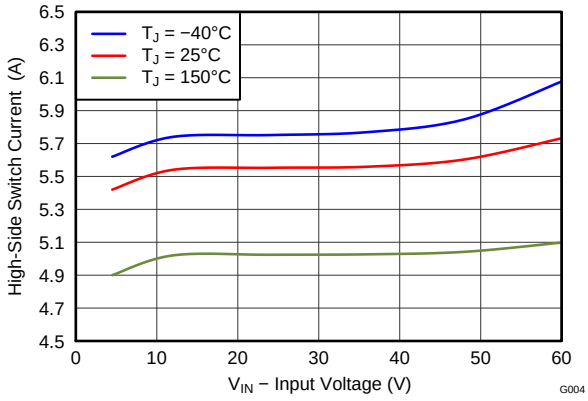


Figure 4. Switch Current Limit vs Input Voltage

Typical Characteristics (continued)

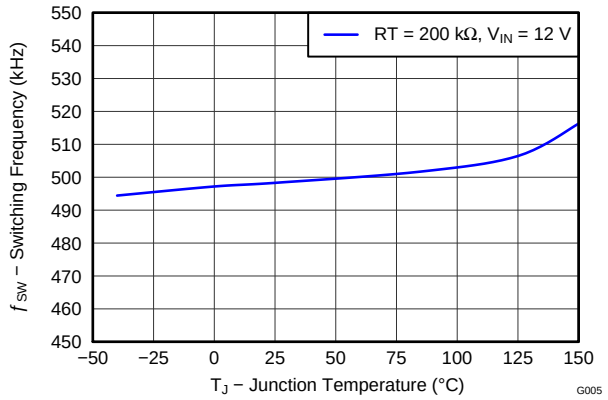


Figure 5. Switching Frequency vs Junction Temperature

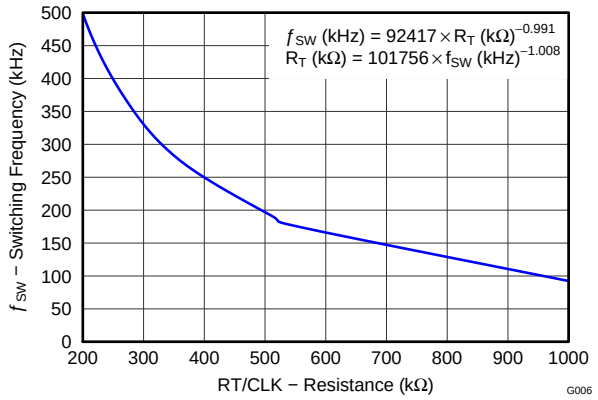


Figure 6. Switching Frequency vs RT/CLK Resistance Low Frequency Range

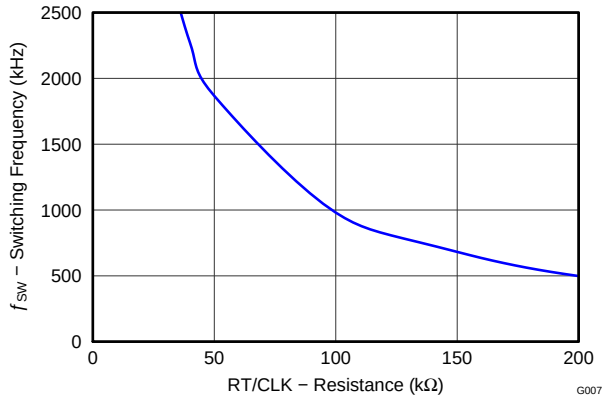


Figure 7. Switching Frequency vs RT/CLK Resistance High Frequency Range

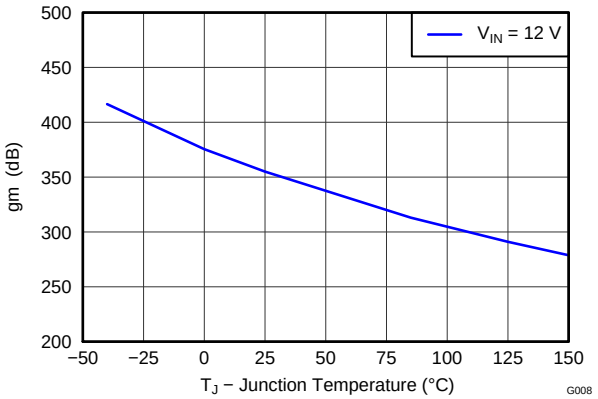


Figure 8. EA Transconductance vs Junction Temperature

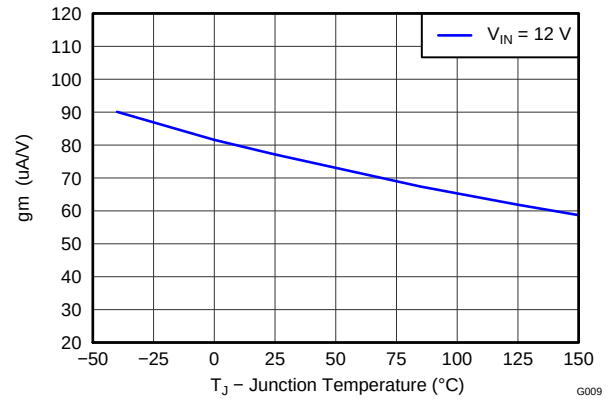


Figure 9. EA Transconductance During Soft-Start vs Junction Temperature

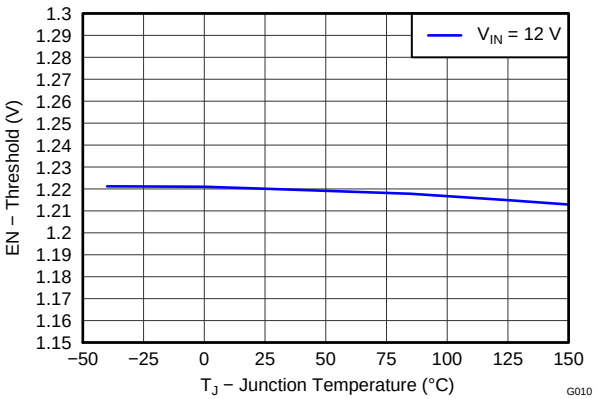


Figure 10. EN Terminal Voltage vs Junction Temperature

Typical Characteristics (continued)

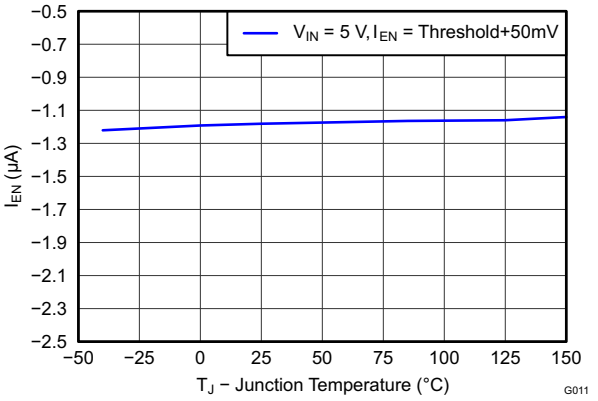


Figure 11. EN Terminal Current vs Junction Temperature

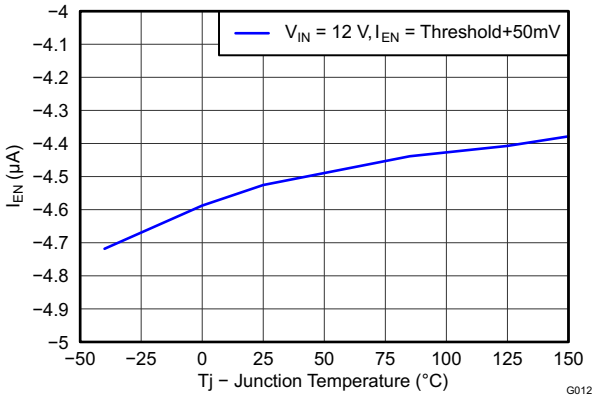


Figure 12. EN Terminal Current vs Junction Temperature

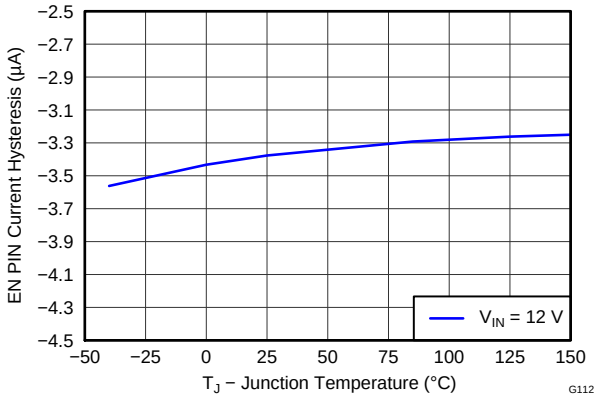


Figure 13. EN Terminal Current Hysteresis vs Junction Temperature

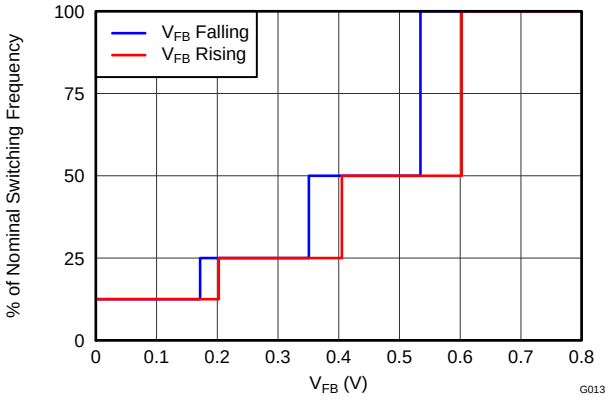


Figure 14. Switching Frequency vs FB

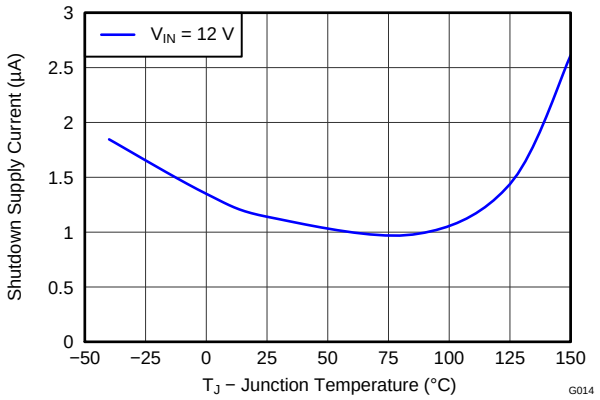


Figure 15. Shutdown Supply Current vs Junction Temperature

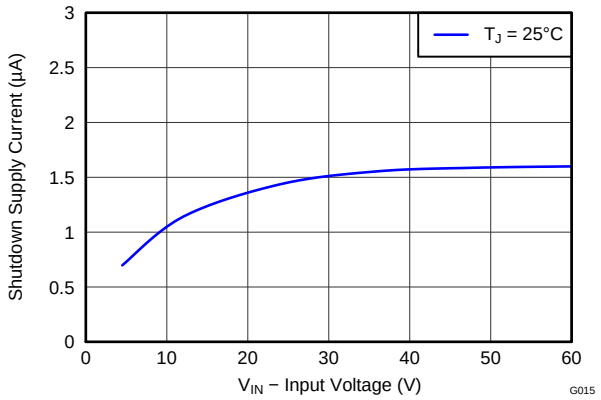


Figure 16. Shutdown Supply Current vs Input Voltage (V_{IN})

Typical Characteristics (continued)

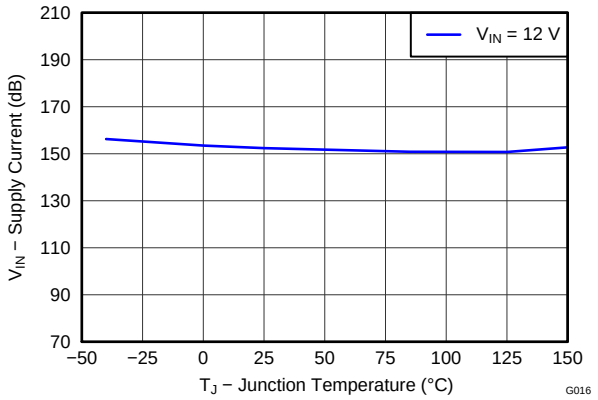


Figure 17. V_{IN} Supply Current vs Junction Temperature

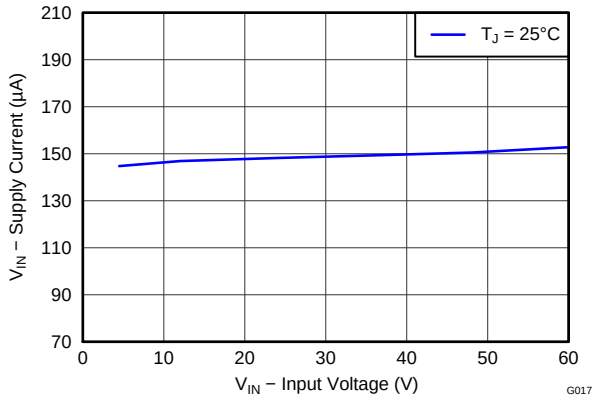


Figure 18. V_{IN} Supply Current vs Input Voltage

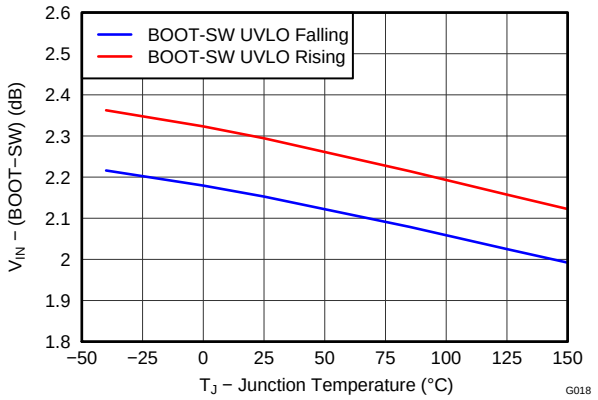


Figure 19. BOOT-SW UVLO vs Junction Temperature

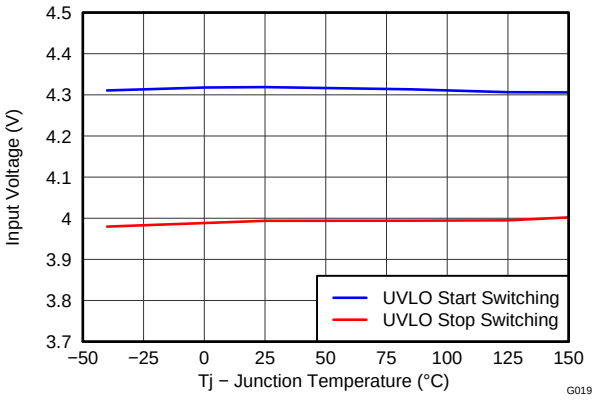


Figure 20. Input Voltage UVLO vs Junction Temperature

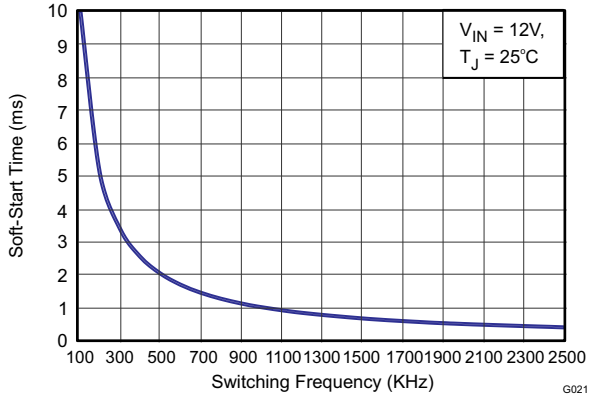


Figure 21. Soft-Start Time vs Switching Frequency

7 Detailed Description

7.1 Overview

The TPS54360 is a 60-V, 3.5-A, step-down (buck) regulator with an integrated high side n-channel MOSFET. The device implements constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation. The wide switching frequency range of 100 kHz to 2500 kHz allows either efficiency or size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground connected to the RT/CLK terminal. The device has an internal phase-locked loop (PLL) connected to the RT/CLK terminal that will synchronize the power switch turn on to a falling edge of an external clock signal.

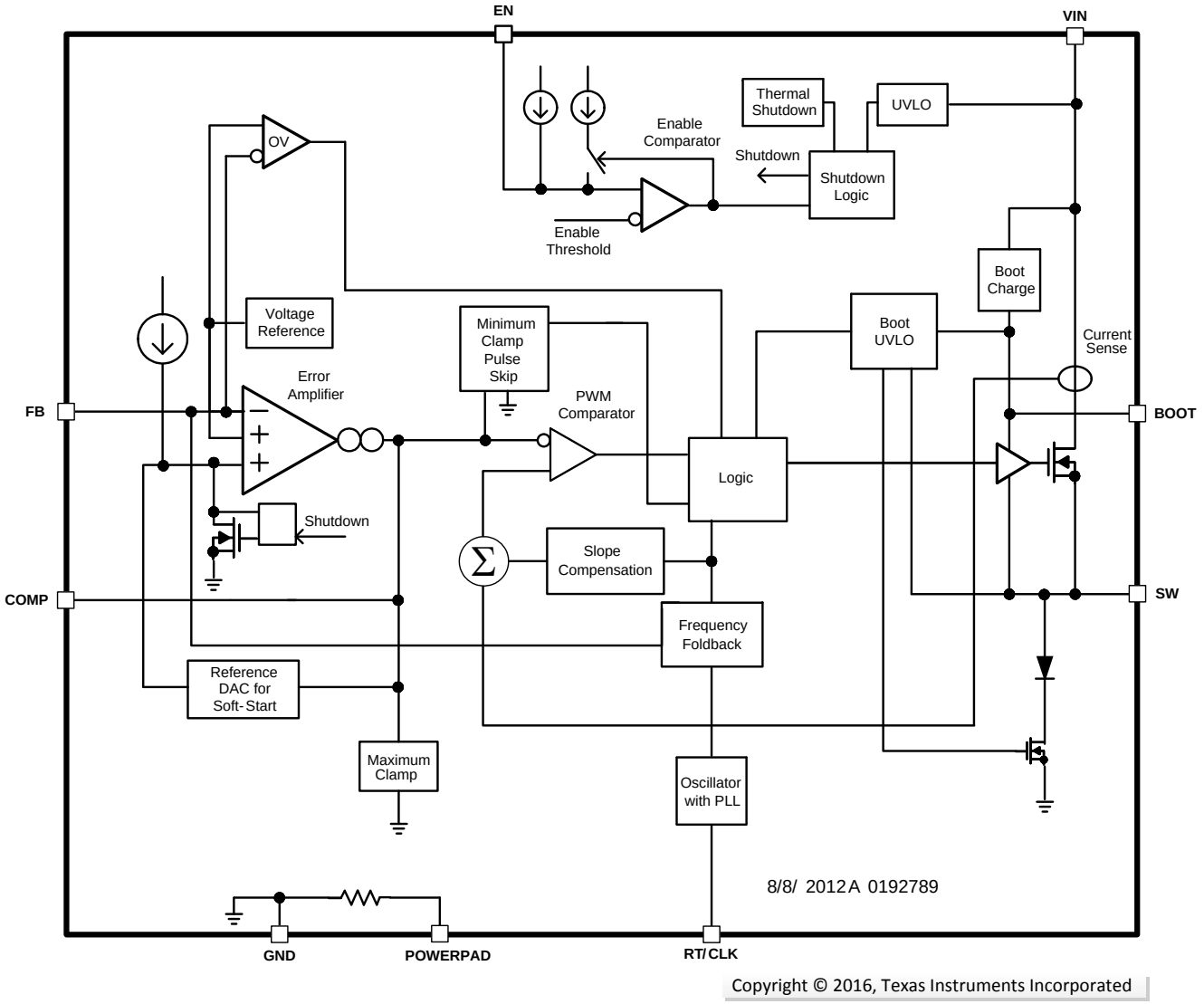
The TPS54360 has a default input start-up voltage of approximately 4.3 V. The EN terminal can be used to adjust the input voltage undervoltage lockout (UVLO) threshold with two external resistors. An internal pull up current source enables operation when the EN terminal is floating. The operating current is 146 μA under no load condition (not switching). When the device is disabled, the supply current is 2 μA.

The integrated 92mΩ high side MOSFET supports high efficiency power supply designs capable of delivering 3.5 amperes of continuous current to a load. The gate drive bias voltage for the integrated high side MOSFET is supplied by a bootstrap capacitor connected from the BOOT to SW terminals. The TPS54360 reduces the external component count by integrating the bootstrap recharge diode. The BOOT terminal capacitor voltage is monitored by a UVLO circuit which turns off the high side MOSFET when the BOOT to SW voltage falls below a preset threshold. An automatic BOOT capacitor recharge circuit allows the TPS54360 to operate at high duty cycles approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The minimum output voltage is the internal 0.8 V feedback reference.

Output overvoltage transients are minimized by an overvoltage transient protection (OVP) comparator. When the OVP comparator is activated, the high side MOSFET is turned off and remains off until the output voltage is less than 106% of the desired output voltage.

The TPS54360 includes an internal soft-start circuit that slows the output rise time during start-up to reduce in-rush current and output voltage overshoot. Output overload conditions reset the soft-start timer. When the overload condition is removed, the soft-start circuit controls the recovery from the fault output level to the nominal regulation voltage. A frequency foldback circuit reduces the switching frequency during start-up and overcurrent fault conditions to help maintain control of the inductor current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The TPS54360 uses fixed frequency, peak current mode control with adjustable switching frequency. The output voltage is compared through external resistors connected to the FB terminal to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output at the COMP terminal controls the high side power switch current. When the high side MOSFET switch current reaches the threshold level set by the COMP voltage, the power switch is turned off. The COMP terminal voltage will increase and decrease as the output current increases and decreases. The device implements current limiting by clamping the COMP terminal voltage to a maximum level. The pulse skipping Eco-mode is implemented with a minimum voltage clamp on the COMP terminal.

7.3.2 Slope Compensation Output Current

The TPS54360 adds a compensating ramp to the MOSFET switch current sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycles greater than 50%. The peak current limit of the high side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

Feature Description (continued)

7.3.3 Pulse Skip Eco-mode

The TPS54360 operates in a pulse skipping Eco-mode at light load currents to improve efficiency by reducing switching and gate drive losses. If the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse skipping current threshold, the device enters Eco-mode. The pulse skipping current threshold is the peak switch current level corresponding to a nominal COMP voltage of 600 mV.

When in Eco-mode, the COMP terminal voltage is clamped at 600 mV and the high side MOSFET is inhibited. Since the device is not switching, the output voltage begins to decay. The voltage control loop responds to the falling output voltage by increasing the COMP terminal voltage. The high side MOSFET is enabled and switching resumes when the error amplifier lifts COMP above the pulse skipping threshold. The output voltage recovers to the regulated value, and COMP eventually falls below the Eco-mode pulse skipping threshold at which time the device again enters Eco-mode. The internal PLL remains operational when in Eco-mode. When operating at light load currents in Eco-mode, the switching transitions occur synchronously with the external clock signal.

During Eco-mode operation, the TPS54360 senses and controls peak switch current, not the average load current. Therefore the load current at which the device enters Eco-mode is dependent on the output inductor value. The circuit in Figure 34 enters Eco-mode at about 24 mA output current. As the load current approaches zero, the device enters a pulse skip mode during which it draws only 146 μA input quiescent current.

7.3.4 Low Dropout Operation and Bootstrap Voltage (BOOT)

The TPS54360 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW terminals provides the gate drive voltage for the high side MOSFET. The BOOT capacitor is refreshed when the high side MOSFET is off and the external low side diode conducts. The recommended value of the BOOT capacitor is 0.1 μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended for stable performance over temperature and voltage.

When operating with a low voltage difference from input to output, the high side MOSFET of the TPS54360 will operate at 100% duty cycle as long as the BOOT to SW terminal voltage is greater than 2.1 V. When the voltage from BOOT to SW drops below 2.1 V, the high side MOSFET is turned off and an integrated low side MOSFET pulls SW low to recharge the BOOT capacitor. To reduce the losses of the small low side MOSFET at high output voltages, it is disabled at 24 V output and re-enabled when the output reaches 21.5 V.

Because the gate drive current sourced from the BOOT capacitor is small, the high side MOSFET can remain on for many switching cycles before the MOSFET is turned off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 100%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low side diode voltage and the printed circuit board resistance.

Equation 1 calculates the minimum input voltage required to regulate the output voltage and ensure normal operation of the device. This calculation must include tolerance of the component specifications and the variation of these specifications at their maximum operating temperature in the application.

$$V_{IN}(\min) = \frac{V_{OUT} + V_F + R_{dc} \times I_{OUT}}{0.99} + R_{DS(on)} \times I_{OUT} - V_F \quad (1)$$

where

- V_F = Schottky diode forward voltage
- R_{dc} = DC resistance of inductor and PCB
- $R_{DS(on)}$ = High-side MOSFET $R_{DS(on)}$

Feature Description (continued)

At heavy loads, the minimum input voltage must be increased to ensure a monotonic start- up. Use Equation 2 to calculate the minimum input voltage for this condition.

$$V_{OUT(max)} = D_{(max)} \times (V_{IN(min)} - I_{OUT(max)} \times R_{DS(on)} + V_F) - V_F + I_{OUT(max)} \times R_{dc}$$

where

- $D_{(max)} \geq 0.9$
- IB2SW = 100 µA
- $t_{SW} = 1 / f_{SW}$(MHz)
- VB2SW = VBOOT + V_F
- VBOOT = (1.41 × V_{IN} – 0.554 – V_F / t_{SW} – 1.847 × 10^3 × IB2SW) / (1.41 + 1 / t_{SW})*
- $R_{DS(on)} = 1 / (–0.3 \times VB2SW^2 + 3.577 \times VB2SW – 4.246)$

*VBOOT is clamped by the IC. If VBOOT calculates to greater than 6 V, set VBOOT = 6 V (2)

7.3.5 Error Amplifier

The TPS54360 voltage regulation loop is controlled by a transconductance error amplifier. The error amplifier compares the FB terminal voltage to the lower of the internal soft-start voltage or the internal 0.8 V voltage reference. The transconductance (gm) of the error amplifier is 350 µA/V during normal operation. During soft-start operation, the transconductance is reduced to 78 µA/V and the error amplifier is referenced to the internal soft-start voltage.

The frequency compensation components (capacitor, series resistor and capacitor) are connected between the error amplifier output COMP terminal and GND terminal.

7.3.6 Adjusting the Output Voltage

The internal voltage reference produces a precise 0.8 V ±1% voltage reference over the operating temperature and voltage range by scaling the output of a bandgap reference circuit. The output voltage is set by a resistor divider from the output node to the FB terminal. It is recommended to use 1% tolerance or better divider resistors. Select the low side resistor R_{LS} for the desired divider current and use Equation 3 to calculate R_{HS}. To improve efficiency at light loads consider using larger value resistors. However, if the values are too high, the regulator will be more susceptible to noise and voltage errors from the FB input current may become noticeable.

$$R_{HS} = R_{LS} \times \left(\frac{Vout - 0.8V}{0.8\ V} \right) \quad (3)$$

7.3.7 Enable and Adjusting Undervoltage Lockout

The TPS54360 is enabled when the VIN terminal voltage rises above 4.3 V and the EN terminal voltage exceeds the enable threshold of 1.2 V. The TPS54360 is disabled when the VIN terminal voltage falls below 4 V or when the EN terminal voltage is below 1.2 V. The EN terminal has an internal pull-up current source, I1, of 1.2 µA that enables operation of the TPS54360 when the EN terminal floats.

If an application requires a higher undervoltage lockout (UVLO) threshold, use the circuit shown in Figure 22 to adjust the input voltage UVLO with two external resistors. When the EN terminal voltage exceeds 1.2 V, an additional 3.4 µA of hysteresis current, Ihys, is sourced out of the EN terminal. When the EN terminal is pulled below 1.2 V, the 3.4 µA Ihys current is removed. This addional current facilitates adjustable input voltage UVLO hysteresis. Use Equation 4 to calculate R_{UVLO1} for the desired UVLO hysteresis voltage. Use Equation 5 to calculate R_{UVLO2} for the desired VIN start voltage.

In applications designed to start at relatively low input voltages (e.g., from 4.5 V to 9 V) and withstand high input voltages (e.g., from 40 V to 60 V), the EN terminal may experience a voltage greater than the absolute maximum voltage of 8.4 V during the high input voltage condition. It is recommended to use a zener diode to clamp the terminal voltage below the absolute maximum rating.

Feature Description (continued)

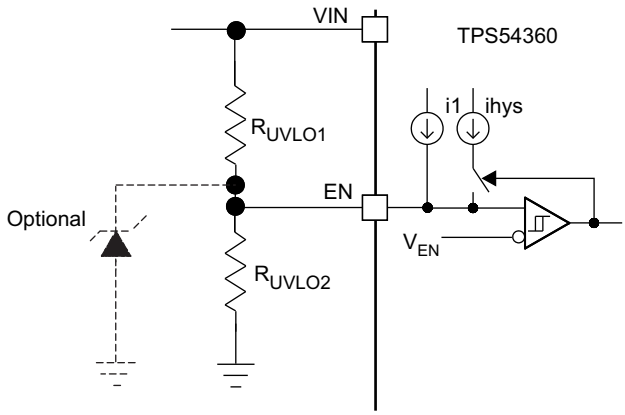


Figure 22. Adjustable Undervoltage Lockout (UVLO)

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (4)$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} \quad (5)$$

7.3.8 Internal Soft-Start

The TPS54360 has an internal digital soft-start that ramps the reference voltage from zero volts to its final value in 1024 switching cycles. The internal soft-start time (10% to 90%) is calculated using Equation 6.

$$t_{SS}(ms) = \frac{1024}{f_{SW}(kHz)} \quad (6)$$

If the EN terminal is pulled below the stop threshold of 1.2 V, switching stops and the internal soft-start resets. The soft-start also resets in thermal shutdown.

7.3.9 Constant Switching Frequency and Timing Resistor (RT/CLK) Terminal)

The switching frequency of the TPS54360 is adjustable over a wide range from 100 kHz to 2500 kHz by placing a resistor between the RT/CLK terminal and GND terminal. The RT/CLK terminal voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 7 or Equation 8 or the curves in Figure 5 and Figure 6. To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the conversion efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 135 ns which limits the maximum operating frequency in applications with high input to output step down ratios. The maximum switching frequency is also limited by the frequency foldback circuit. A more detailed discussion of the maximum switching frequency is provided in the next section.

$$R_T\ (k\Omega) = \frac{101756}{f\text{sw}\ (kHz)^{1.008}} \quad (7)$$

$$f\text{sw}\ (kHz) = \frac{92417}{RT\ (k\Omega)^{0.991}} \quad (8)$$