Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV$_{DSS}$ / BV$_{DGS}$	R$_{DS(ON)}$ (max)	I$_{D(ON)}$ (min)	Order Number / Package	
			TO-92	Die[†]
-40V	8.0Ω	-0.5A	VP0104N3	—
-60V	8.0Ω	-0.5A	VP0106N3	—
-90V	8.0Ω	-0.5A	VP0109N3	VP0109ND

Features

❏ Free from secondary breakdown

❏ Low power drive requirement

❏ Ease of paralleling

❏ Low C$_{ISS}$ and fast switching speeds

❏ Excellent thermal stability

❏ Integral Source-Drain diode

❏ High input impedance and high gain

❏ Complementary N- and P-channel devices

Applications

❏ Motor controls

❏ Converters

❏ Amplifiers

❏ Switches

❏ Power supply circuits

❏ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

|	
Drain-to-Source Voltage	BV$_{DSS}$
Drain-to-Gate Voltage	BV$_{DGS}$
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option

S G D

TO-92

Note: See Package Outline section for dimensions.
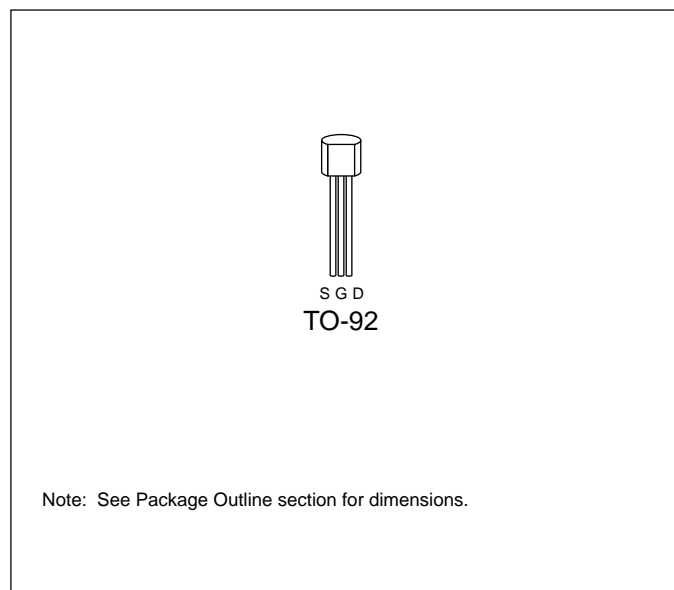
Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	-0.25A	-0.8A	1.0W	125	170	-0.25A	-0.8A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0109	-90			V	I_D = -1.0mA, V_{GS} = 0V
		VP0106	-60				
		VP0104	-40				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			5.8	6.5	mV/°C	I_D = -1.0mA, V_{GS} = V_{DS}
I_{GSS}	Gate Body Leakage			-1.0	-100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current				-10	μA	V_{GS} = 0V, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-0.15	-0.25		A	V_{GS} = -5V, V_{DS} = -25V
			-0.50	-1.2			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			11	15	Ω	V_{GS} = -5V, I_D = -0.1A
				6.0	8.0		V_{GS} = -10V, I_D = -0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.55	1.0	%/°C	V_{GS} = -10V, I_D = -0.5A
G_{FS}	Forward Transconductance		150	190		m℧	V_{DS} = -25V, I_D = -0.5A
C_{ISS}	Input Capacitance			45	60	pF	V_{GS} = 0V, V_{DS} = -25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			22	30		
C_{RSS}	Reverse Transfer Capacitance			3	8		
$t_{d(ON)}$	Turn-ON Delay Time			4	6	ns	V_{DD} = -25V I_D = -0.5A R_{GEN} = 25Ω
t_r	Rise Time			3	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			8	12		
t_f	Fall Time			4	10		
V_{SD}	Diode Forward Voltage Drop			-1.2	-2.0	V	I_{SD} = -1.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time			400		ns	I_{SD} = -1.0A, V_{GS} = 0V

Notes:
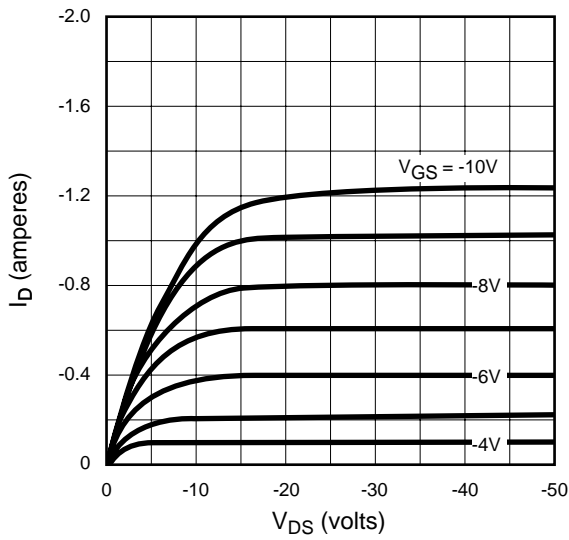1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit
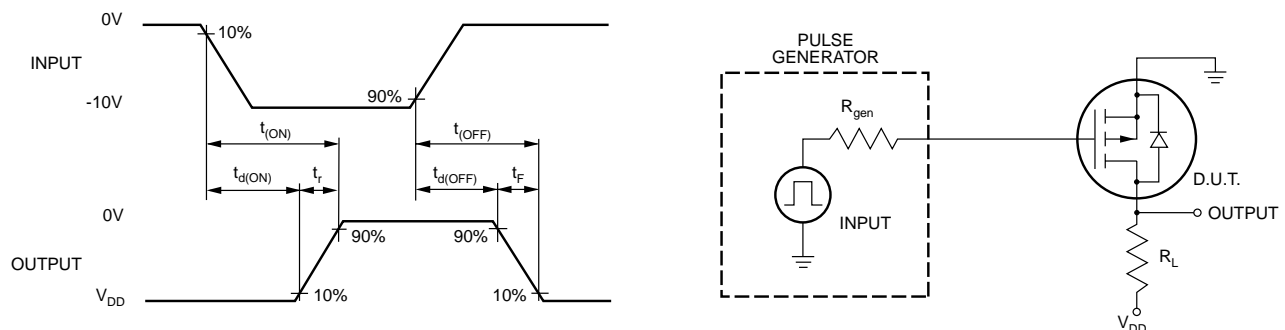
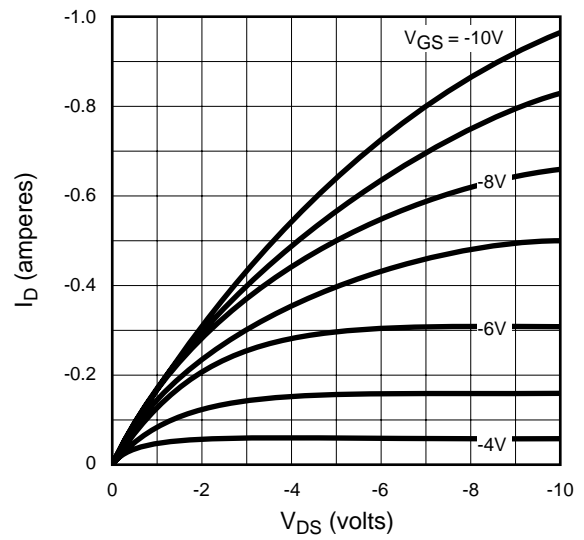# Typical Performance Curves

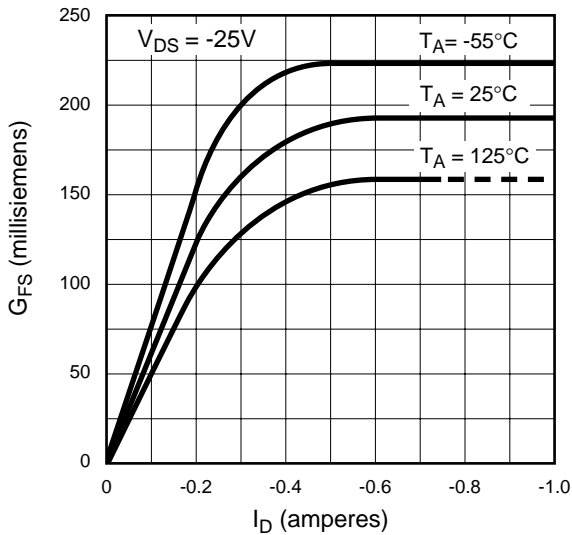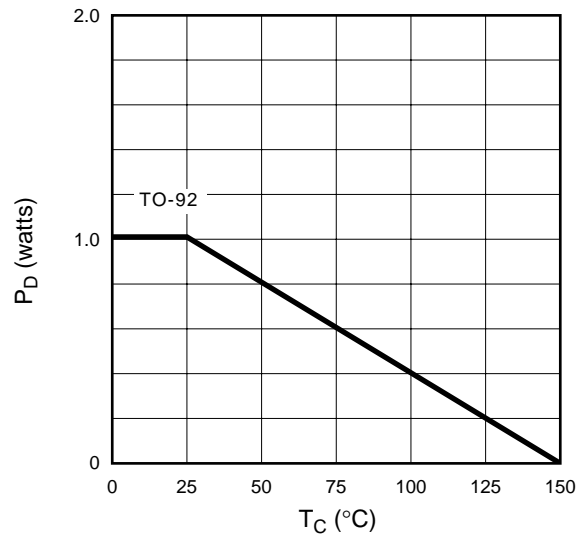### Output Characteristics

$V_{GS} = -10V$

-8V

-6V

-4V

V_{DS} (volts)

I_D (amperes)

Saturation Characteristics

$V_{GS} = -10V$

-8V

-6V

-4V

V_{DS} (volts)

I_D (amperes)

Transconductance vs. Drain Current

$V_{DS} = -25V$

$T_A = -55°C$

$T_A = 25°C$

$T_A = 125°C$

G_{FS} (millisiemens)

I_D (amperes)

Power Dissipation vs. Case Temperature

TO-92

P_D (watts)

T_C (°C)

Maximum Rated Safe Operating Area

TO-92(DC)

$T_C = 25°C$

I_D (amperes)

V_{DS} (volts)
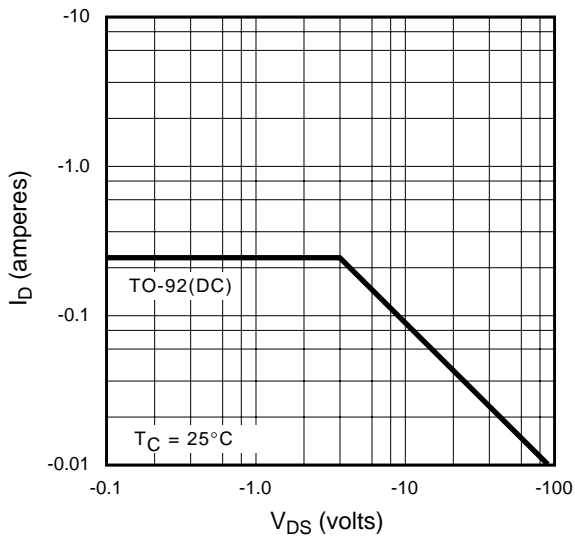
Thermal Response Characteristics

TO-92
$P_D = 1W$
$T_C = 25°C$

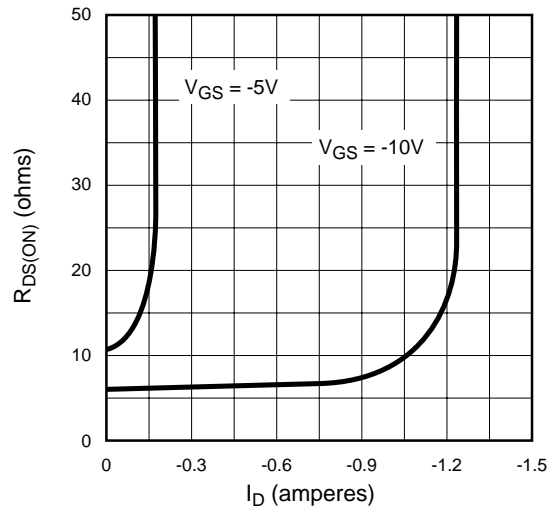Thermal Resistance (normalized)

t_p (seconds)

3
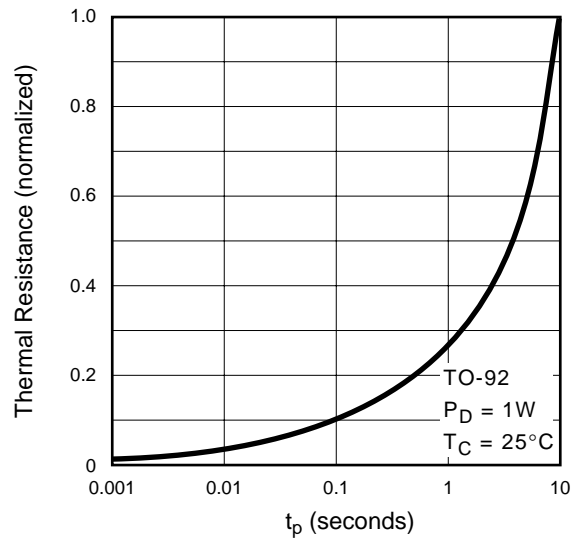
Typical Performance Curves

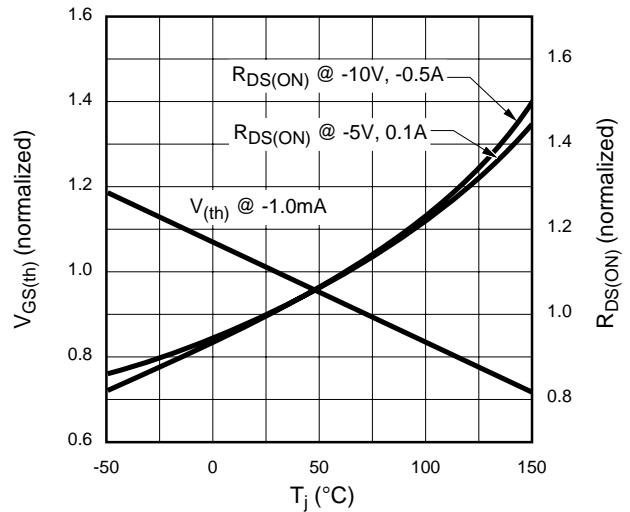### BV$_{DSS}$ Variation with Temperature
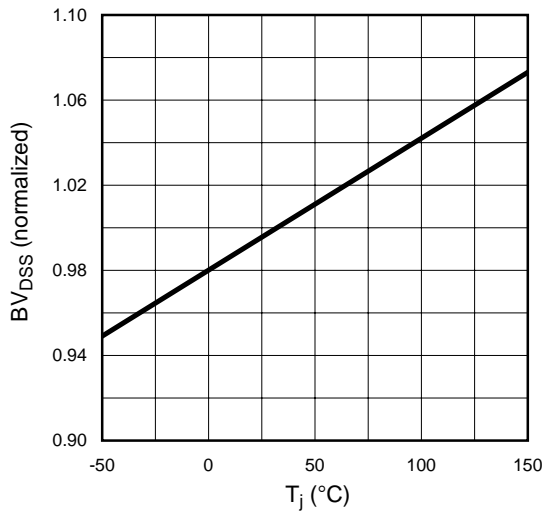
On-Resistance vs. Drain Current

Transfer Characteristics
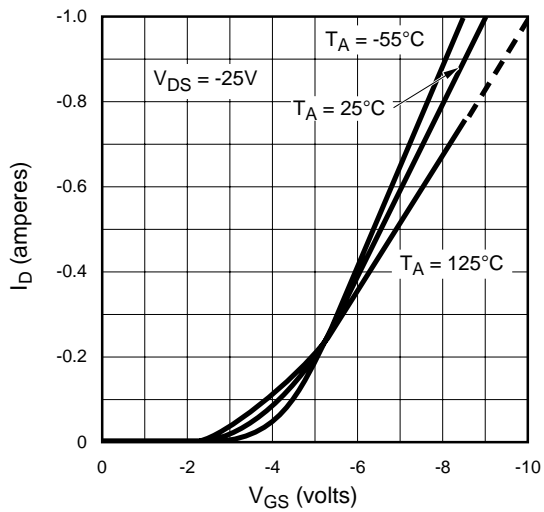
V$_{(th)}$ and R$_{DS}$ Variation with Temperature

Capacitance vs. Drain-to-Source Voltage
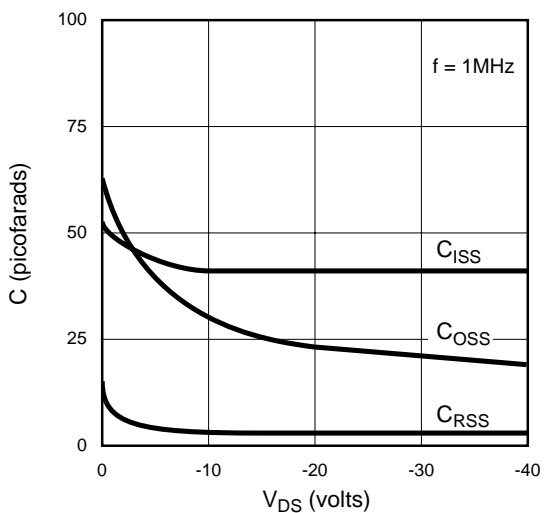
Gate Drive Dynamic Characteristics

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